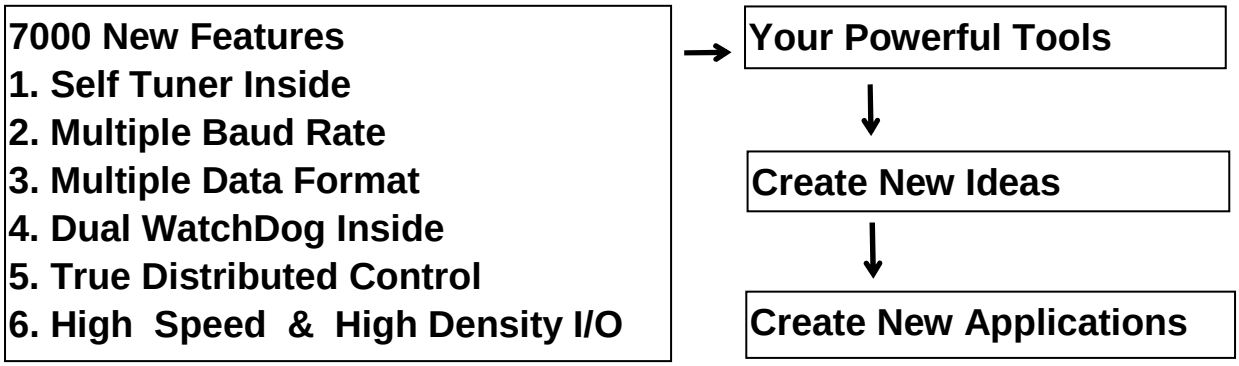
I/O Expansion Bus for 7188X/7188E

User's Manual (Volume 1)



Warranty

All products manufactured by ICP DAS are warranted against defective materials for a period of one year from the date of delivery to the original purchaser.

Warning

ICP DAS assume no liability for damages consequent to the use of this product. ICP DAS reserves the right to change this manual at any time without notice. The information furnished by ICP DAS is believed to be accurate and reliable. However, no responsibility is assumed by ICP DAS for its use, not for any infringements of patents or other rights of third parties resulting from its use.

Copyright

Trademark

The names used for identification only may be registered trademarks of their respective companies.

Table of Contents

1. Introduction

Even though the 7000 family is so powerful, there are some applications chart cannot be solved, such as:

- High speed applications
- Special hardware requirement applications
- Special software requirement applications
- Combine special hardware & software applications

So we developed an I/O expansion bus in the 7188X/7521/7188E family to solve all these applications above. The I/O expansion bus can be used to implement various I/O functions such as D/I, D/O, A/D, D/A, Timer/Counter, UART, flash memory, battery backup SRAM, AsicKey & other I/O functions. **Nearly all kinds of I/O functions can be implemented in this bus.**

The I/O expansion bus includes serial & parallel interface. The parallel interface is very similar to an ISA bus, so the user can move the old ISA bus design to the I/O expansion bus with very little modification. The power consumption table is given as follows:

	7188XC	**7188XB**	**7188EX**	**Note 1:** **Power consumption of 7-SEG LED is 140 mA** **For example: 7188XCD=140+140=280 So I/O=550-280=270 mA max.**
CPU Module	140mA@5V	260mA@5V	290mA@5V	
I/O Expansion Board	410mA@5V	290mA@5V	260mA@5V	
Total Max.	550 mA@5V	550 mA@5V	550 mA@5V	

- Refer to CD\napdos\7188x\manual\hardware**iobus2_e.pdf** for more I/O expansion boards.
- Refer to CD\napdos\7188x\manual\hardware**X-performance** for more performance information about I/O expansion boards.
- The **7188XA** supports I/O expansion bus but does not support user defined pins, so the 7188XA only supports X002 & X600 series.
- The 7522/7523/7188EA does not support I/O expansion buses.

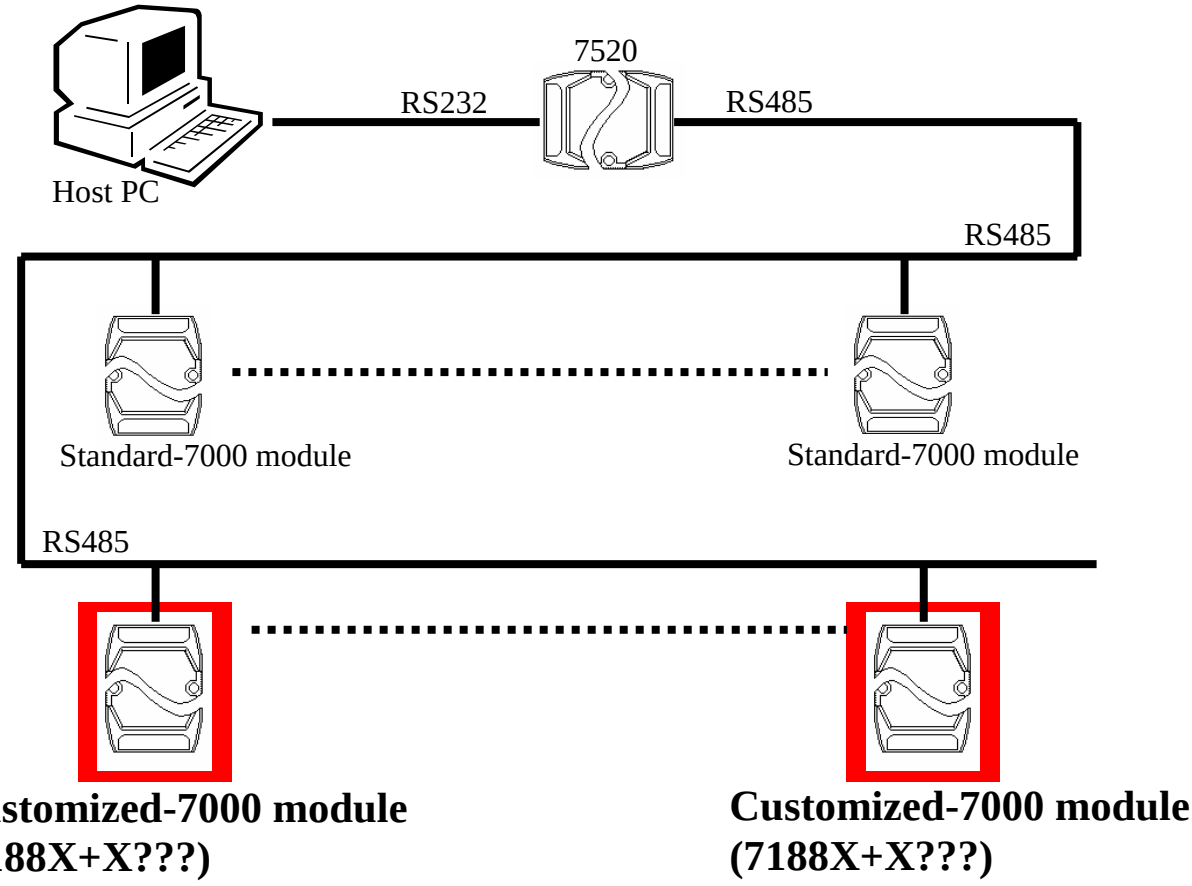
The I/O pins of serial bus are programmable. They can be programmed as D/I, or D/O. Some pins can be configured to D/I or D/O or timer input or timer output. There are many serial interface devices today. The features of these serial devices are given as follows:

- Smaller size compared to parallel devices
- Lower cost compared to parallel devices
- Easier to design for isolation application

The serial interface of an I/O expansion bus can link to these serial devices very easily. The combination of serial & parallel interface makes the I/O expansion bus very easy & powerful for various industry applications. These are many design examples given in this manual and all hardware circuit & software driver sources are OPENING for all user. From these examples, the users can buy these examples or modify them for their special requirements. The system design steps are given as follows:

Step 1: List all functions required.
Step 2: For all functions, go to step 3. If all functions are solved → STOP.
Step 3: If this function can be solved by the 7000 module → Go to step 2 for next function.
Step 4: If this function can be solved by 7188X+X??? → Go to step 2 for next function.
Step 5: Now user must design special hardware on the I/O expansion bus.
Step 6: User writes their special software driver based on this new hardware.
Step 7: Refer to **"7521/7522/7523 Software User's manual"** for firmware. Modify & download this firmware into the CPU module, this module now will work as a customized 7000 module.
Step 8: Go to step 2 for next function.

After the above steps, user can combine the **standard-7000 modules** & **customized-7000 modules** to solve all applications in the same RS-485 network. This customized solution diagram is given as follows:



The design of a I/O Expansion Bus make the idea of a“Customized-7000 Module” come true. The features of a“Customized-7000 Module” are given as follows:

- **7188X+X??? → Single module solution → “Customized-7000 Module”**
- 7000 compatible command sets & RS-485 networking
- Easy hardware/software interface for users to design & manufacture their special hardware & software
- Time-to-market ODM solution for user’s special requirements (any high speed, complex or combined functions of D/I/O, A/D, D/A, ….., etc.)
- Robust, stable, flexible, time-to-market & cost-effective total solution.

Some customized-7000 modules are available as follows:

- IKIT-09: Long Time Data Logger=7188XBD+X800
- IKIT-10: Long Time 7000 Logger=7188XBD+X6??
- IKIT-11: Analog Signal Controller=7188XBD+X801
- IKIT-12: Arbitrary Waveform Generator=7188XCD+X300
- More customized-7000 modules will be ready in the near future

1.1 Software Installation & Demo Programs

Refer to Sec. 1.1 of "7521/7522/7523 Software User's Manual" for software installation. The software driver will be updated frequently. Please refer to www.icpdas.com or www.icpdas.com.tw for user manual & software driver download.

After the software is installed in the hard disk, the demo program will be available as follows: (assume install in C:\7188XC)

C:\7188xc\demo\ioexpbus*.* → demo program for I/O Expansion Bus
C:\7188xc\demo\ioexpbus\X200*.* → demo program for X200
C:\7188xc\demo\ioexpbus\X300*.* → demo program for X300
C:\7188xc\demo\ioexpbus\X301*.* → demo program for X301
……
……
C:\7188xc\demo\ioexpbus\X500*.* → demo program for X500
……
……
The source code of firmware is given as following:
C:\7188xc\demo\7521*.* → firmware source code for 7521
C:\7188xc\demo\7522*.* → firmware source code for 7522
C:\7188xc\demo\7523*.* → firmware source code for 7523
C:\7188xc\demo\7521ODM1*.* → firmware source code for ODM1
C:\7188xc\demo\7521ODM2*.* → firmware source code for ODM2
C:\7188xc\demo\7521ODM3*.* → firmware source code for ODM3
C:\7188xc\demo\7521ODM4*.* → firmware source code for ODM4
C:\7188xc\demo\7522ODM5*.* → firmware source code for ODM5

User can modify these firmwares to fit his special requirements.

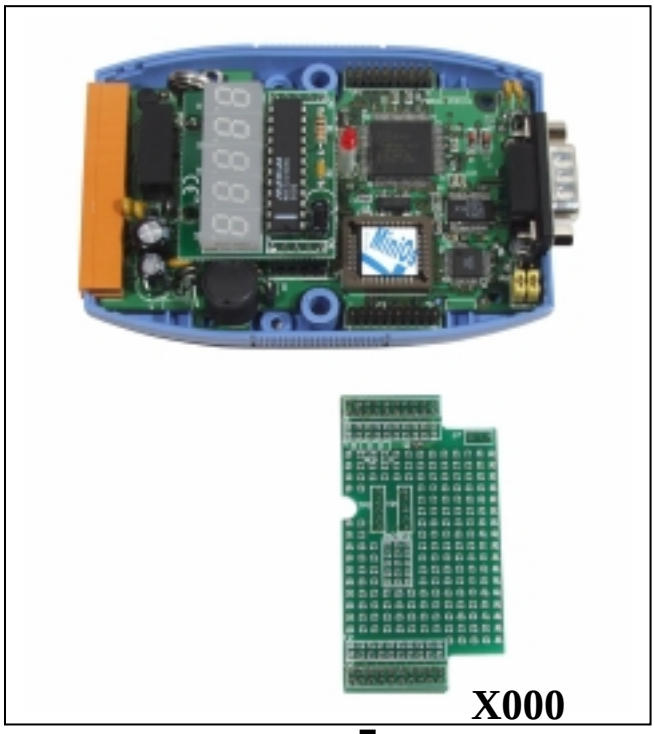
More I/O Expansion Boards will be available in the future. The software & user's manual will be given in our web site. The user's manual for new I/O Expansion Boards will be given as following:

C:\7188xc\newioexp.pdf → user's manual for new I/O Expansion Boards.

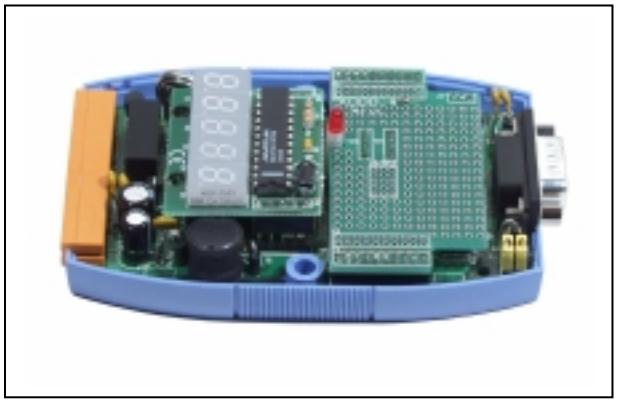
1.2 Mounting of I/O Expansion Bus

1.2.1 Minimal mounting with 7-SEG display

Before mounting:

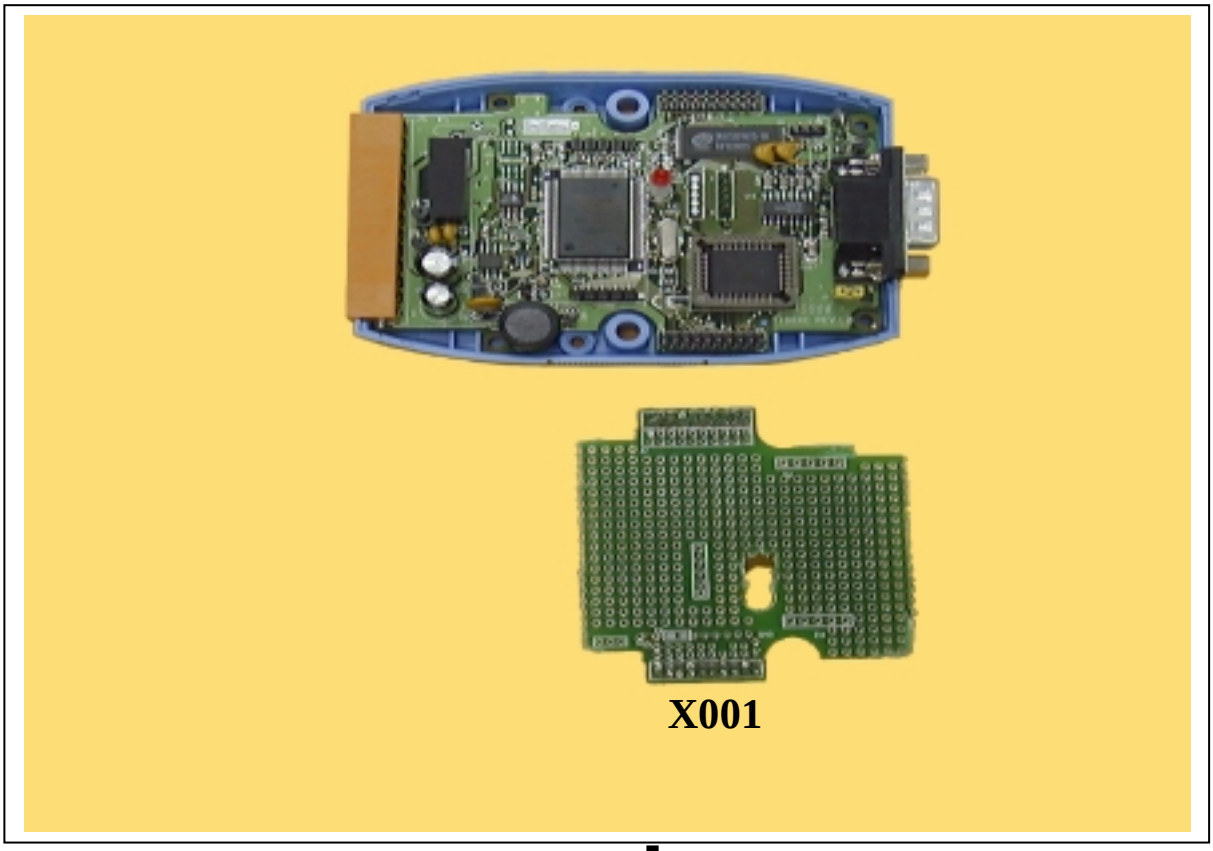


After mounting:

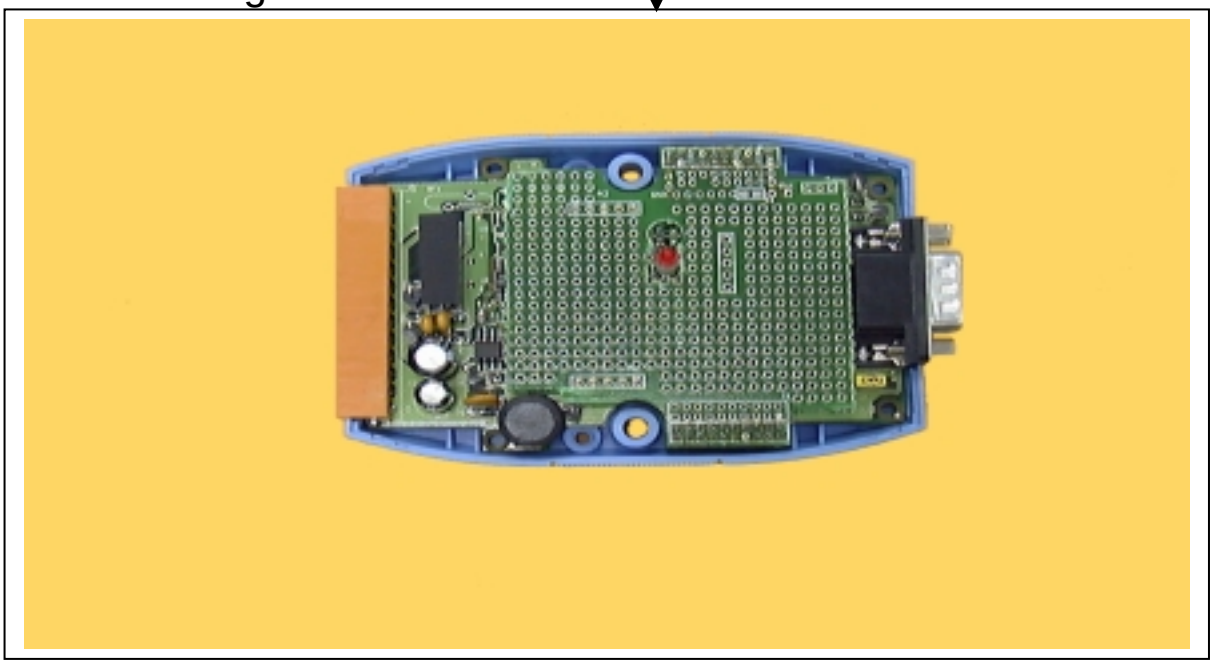


1.2.2 Medium mounting without 7-SEG display

Before mounting:

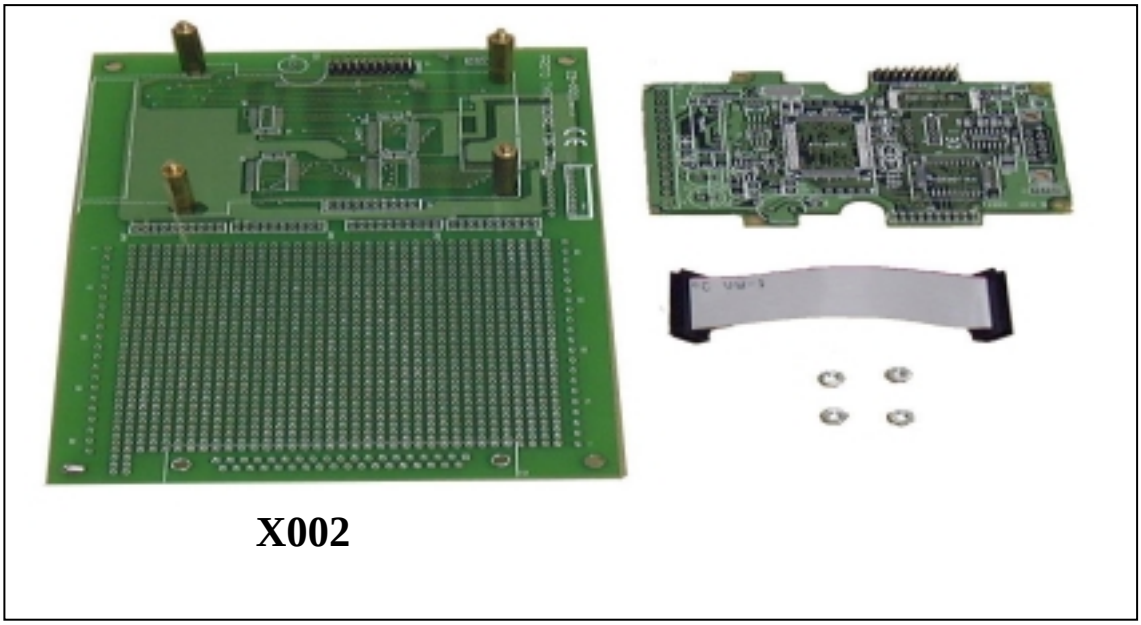


After mounting:

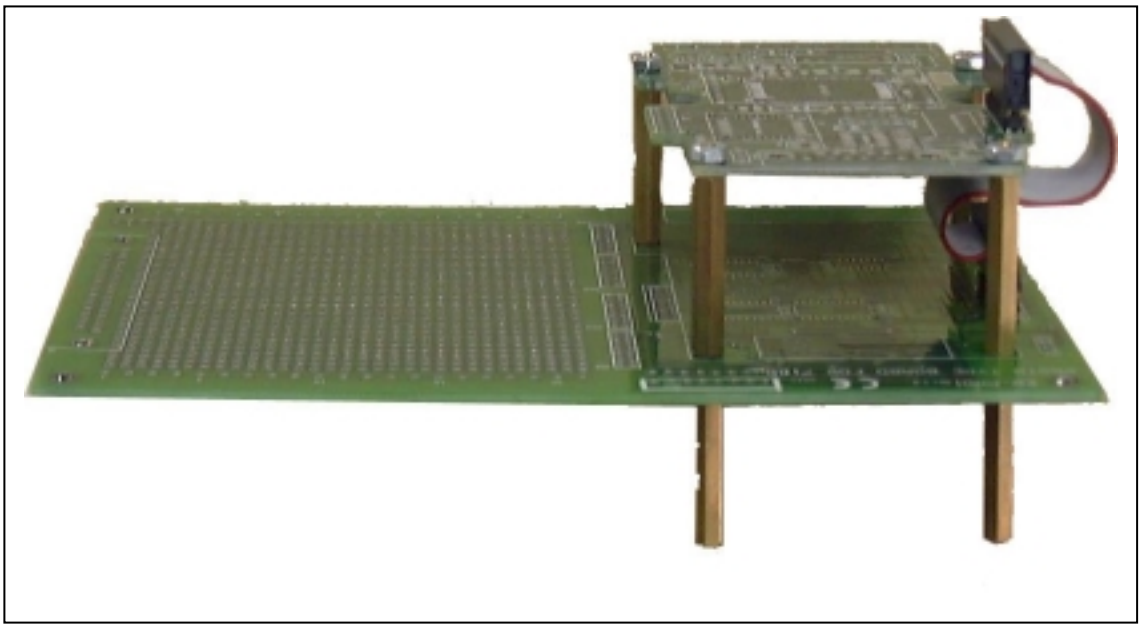


1.2.3 Mounting without CASE

Before mounting:

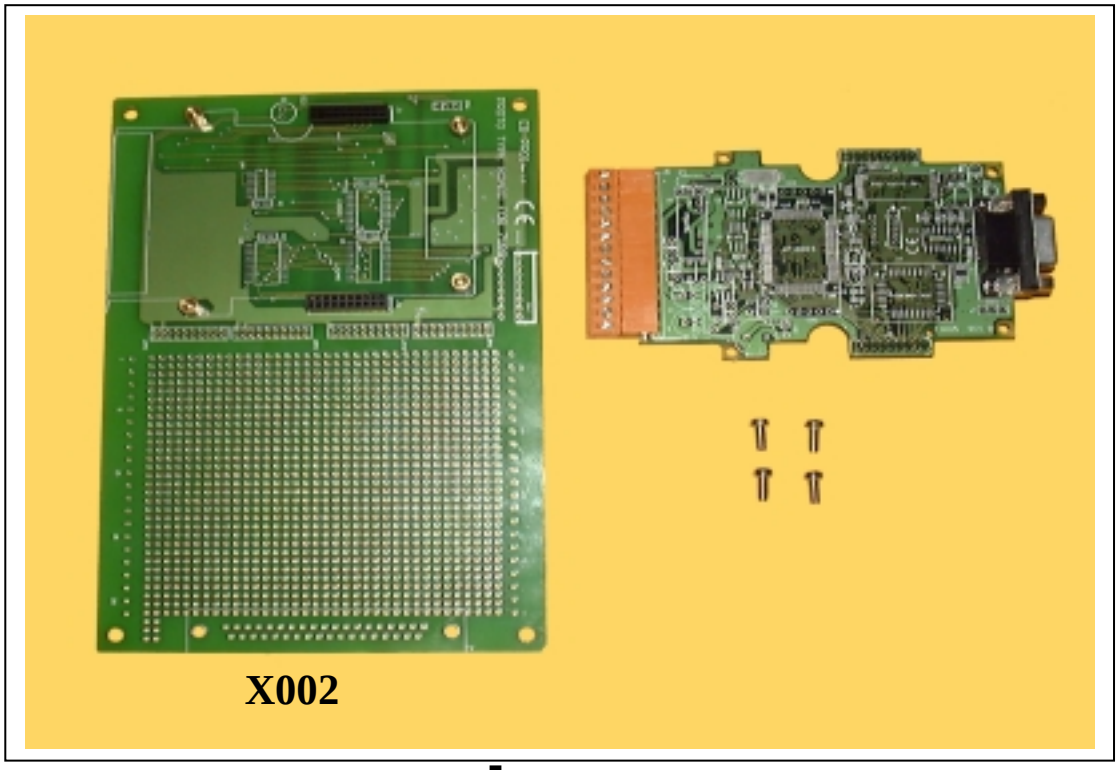


After mounting:

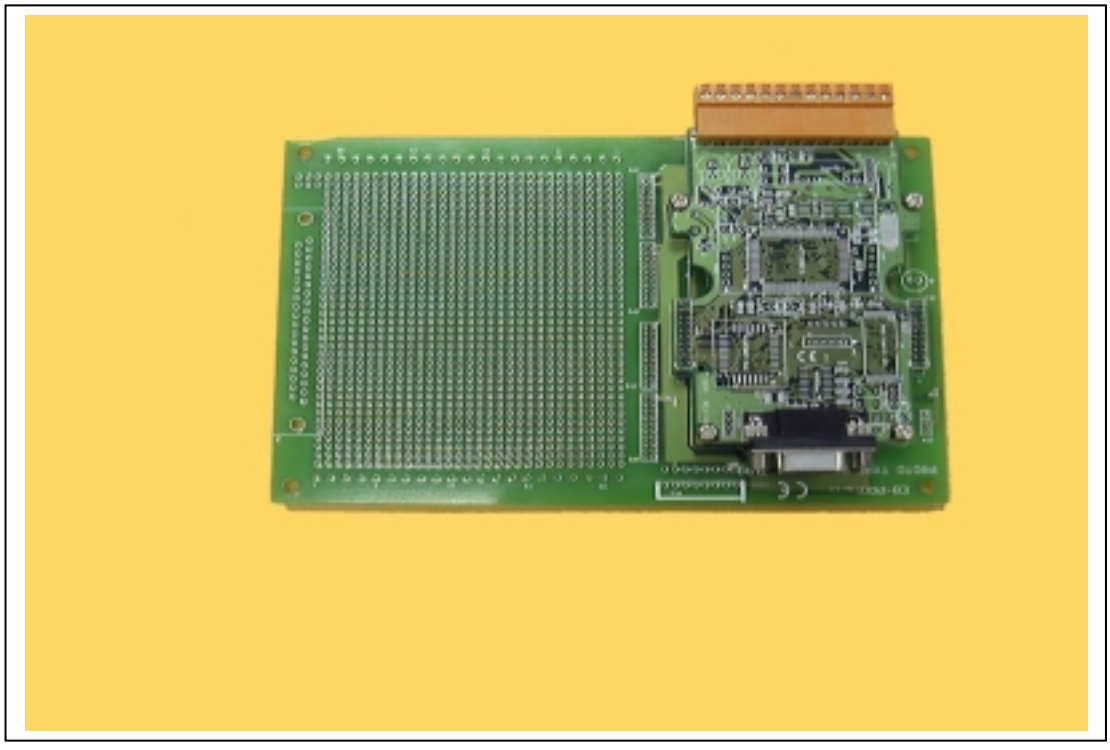


1.2.4 ODM mounting without CASE

Before mounting:



After mounting:



2. I/O Expansion Bus

The I/O expansion bus of 7188X/7188E series can be divided into 3 groups as follows:

1. Power supply & reset signals: VCC, GND, RESET, /RESET
2. Parallel Bus:
   - System clock: CLOCKA
   - Asynchronous ready control: ARDY
   - Address bus: A0 ~ A6, A7 (7188XC & 7521 series without A7)
   - Data bus: D0 ~ D7
   - Interrupt control: INT0, INT1, INT4 (7188XC & 7521 series without INT4)
   - Chip select & read/write strobe: /CS, /WR, /RD
3. Serial Bus: TO_0, TO_1, TI_0, TI_1, SCLK, DIO9, DIO4, DIO14

- Refer to CD\napdos\7188x\manual\hardware**iobus2_e.pdf** for more I/O expansion modules
- Refer to CD\napdos\7188x\manual\hardware**X-performance** for more performance information about I/O expansion boards.
- The **7188XA** supports I/O expansion bus but does not support user defined pins, so the 7188XA only supports X002 & X600 series.
- The 7522/7523/7188EA does not support I/O expansion buses.

2.1 Definition

The definition of I/O expansion bus is given as follows:

J1 pin definition & description:

No	Name	Description
1	GND	Ground of PCB
2	GND	Ground of PCB
3	CLOCKA	Synchronous clock output of CPU
4	ARDY	Asynchronous ready input (level sensitive, OPEN=ready)
5	INT0	Interrupt request input of channel 0 (asynchronous, active high)
6	INT1	Interrupt request input of channel 1 (asynchronous, active high)
7	VCC	Power supply of PCB
8	RESET	Power up reset pulse (active high)
9	GND	Ground of PCB
10	/RESET	Power up reset pulse (active low)
11	TO_0	Timer output 0 of CPU (can be used as programmable D/I/O)
12	TO_1	Timer output 1 of CPU (can be used as programmable D/I/O)
13	TI_0	Timer input 0 of CPU (can be used as programmable D/I/O)
14	TI_1	Timer input 1 of CPU (can be used as programmable D/I/O)
15	SCLK	Common serial clock output of 7188 series
16	DIO9	Programmable D/I/O bit
17	DIO4	Programmable D/I/O bit
18	DIO14	Programmable D/I/O bit
19	VCC	Power supply of PCB
20	VCC	Power supply of PCB

- CLOCKA: 20.2752M Hz for 7188XC, 40M Hz for 7188XA, 7188XB & 7188EA/B/C/X
- ARDY: let this pin OPEN for no wait states applications
- INT0, INT1: let these two pins OPEN for no interrupt applications
- TO_0, TO_1: can be used as CPU's timer output or programmable D/I/O
- TI_0, TI_1: can be used as CPU's timer input or programmable D/I/O
- DIO4, DIO9, DIO14: programmable D/I/O bit
- SCLK: the 7188X/7188E series use this signal as a CLOCK source to drive all on-board serial devices, so it is always be programmed as D/O. Change this signal to other configuration will cause serious errors. User can use this signal to drive external serial devices without any side effects.

J2 pin definition & description:

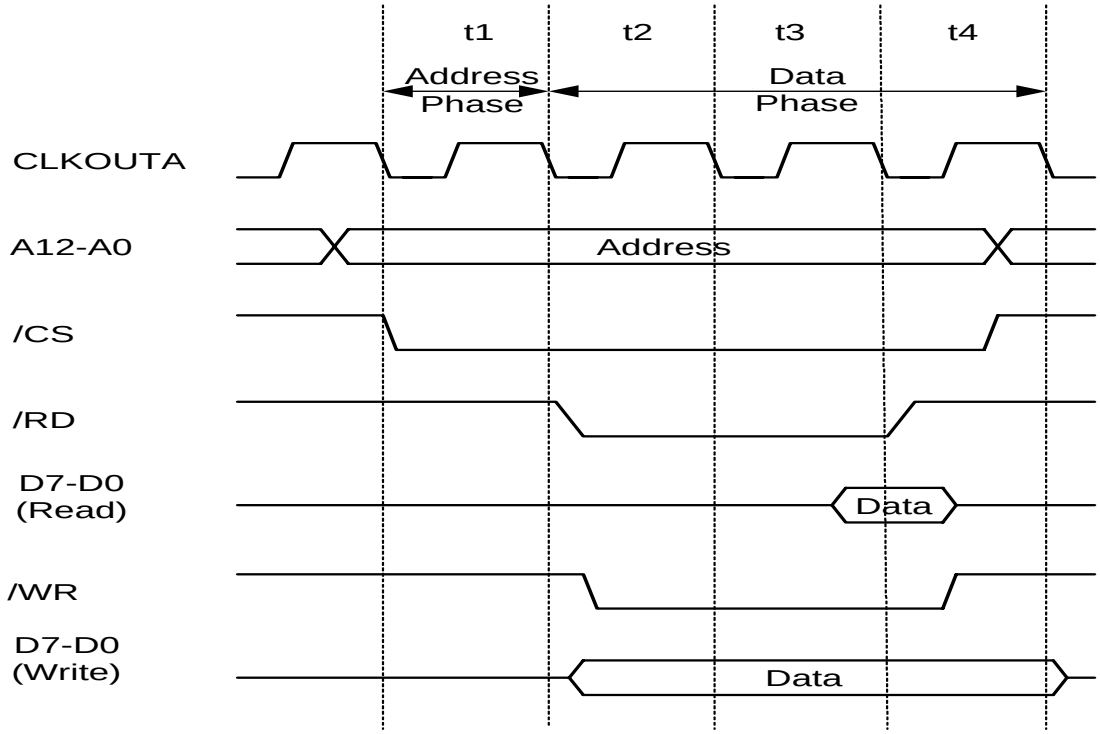
No	Name	Description
1	A0	Address bus
2	D0	Data bus
3	A1	Address bus
4	D1	Data bus
5	A2	Address bus
6	D2	Data bus
7	A3	Address bus
8	D3	Data bus
9	A4	Address bus
10	D4	Data bus
11	A5	Address bus
12	D5	Data bus
13	A6	Address bus
14	D6	Data bus
15	A7 or N/C	**This pin is reserved & must be N/C for 7188XC & 7521 series**
16	D7	Data bus
17	INT4 or N/C	Interrupt request input of channel 4(asynchronous, active high), **this pin is reserved & must be N/C for 7188XC & 7521 series**
18	/WR	Write strobe output (synchronous, active low)
19	/CS	Chip select output (synchronous, active low)
20	/RD	Read strobe output (synchronous, active low)

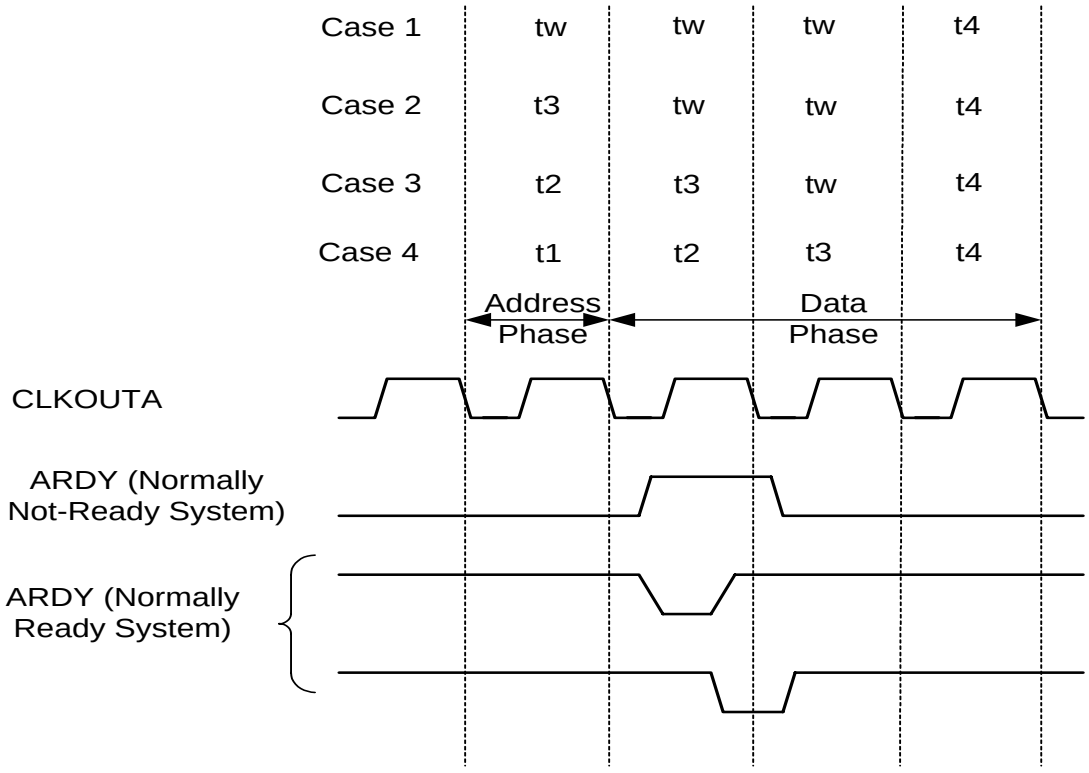
- Address bus (output): A0 ~ A6, A7
- Data Bus (tri-state, bi-direction): D0 to D7
- INT4: let this pin OPEN for no interrupt applications
- /CS, /RD, /WR: These 3 signals will synchronous to CLOCKA (in J1.3) & asynchronous to ARDY (J1.4)
- The CS\ will be active if program input/output from I/O address 0 to 0xff.
- **The pin_15 & pin_17 are reserved by 7188XC & 7521 series; user must left these two pins N/C for 7188XC & 7521 series.**

- The **7188XA** supports I/O expansion bus but does not support user defined pins, so the 7188XA only supports X002 & X600 series.
- The 7522/7523/7188EA does not support I/O expansion buses.

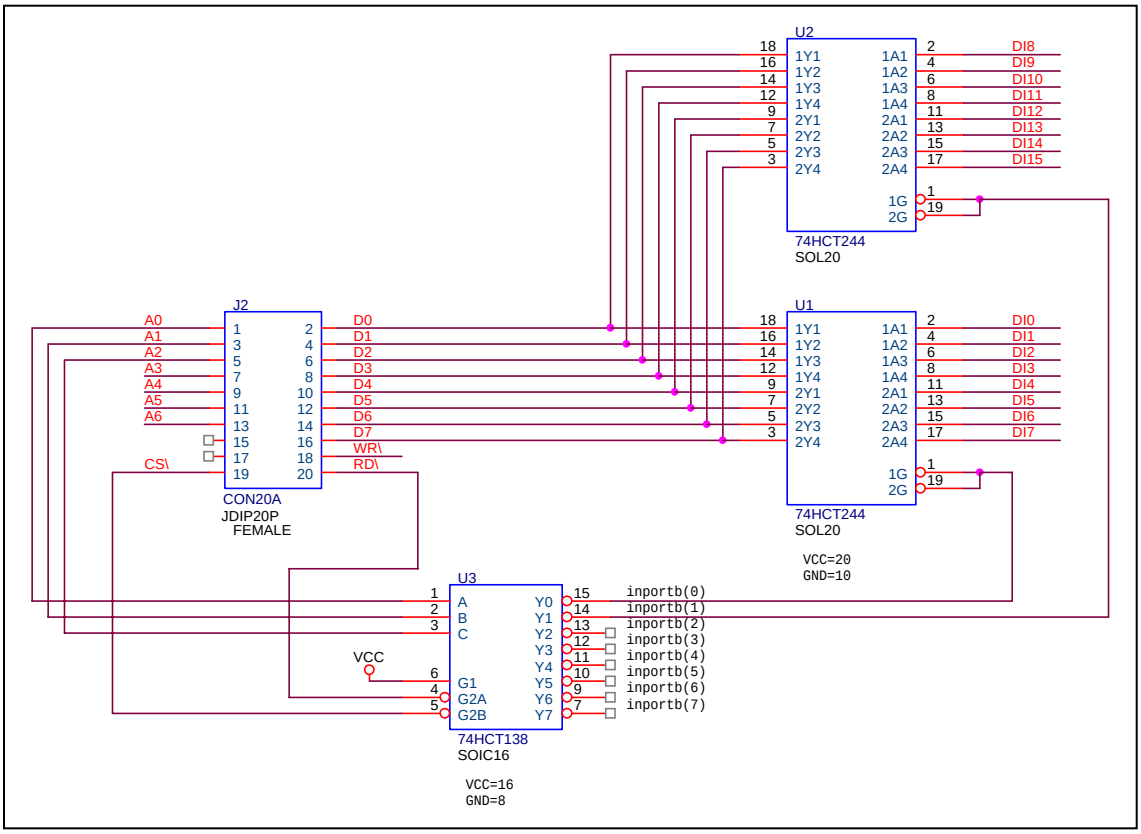
Parallel Bus

2.2.1 Timing Diagram





2.2.2 Address decode & D/I CKT



The CS\ will be active if program input/output from I/O address BASE+0 to BASE+0xff.

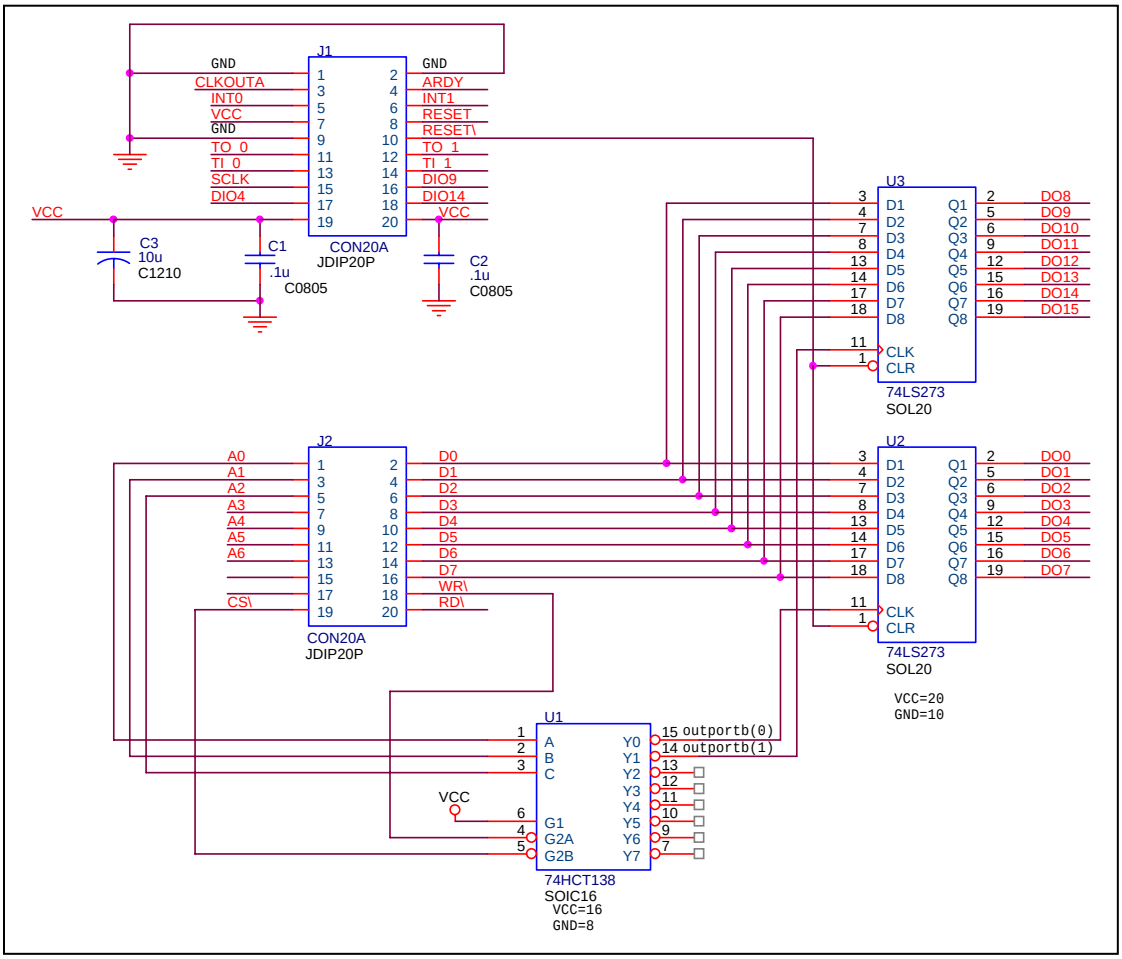
Read DI 0 to 7 → DI_0_7=inportb (BASE+0);

Read DI 8 to 15 → DI_8_15=inportb (BASE+1);

The power-up default value of BASE is 0.

It is **not** recommended to change the value of BASE from 0 to another value.

2.2.3 Address decode & D/O CKT



The CS\ will be active if program input/output from I/O address BASE+0 to BASE+0xff.

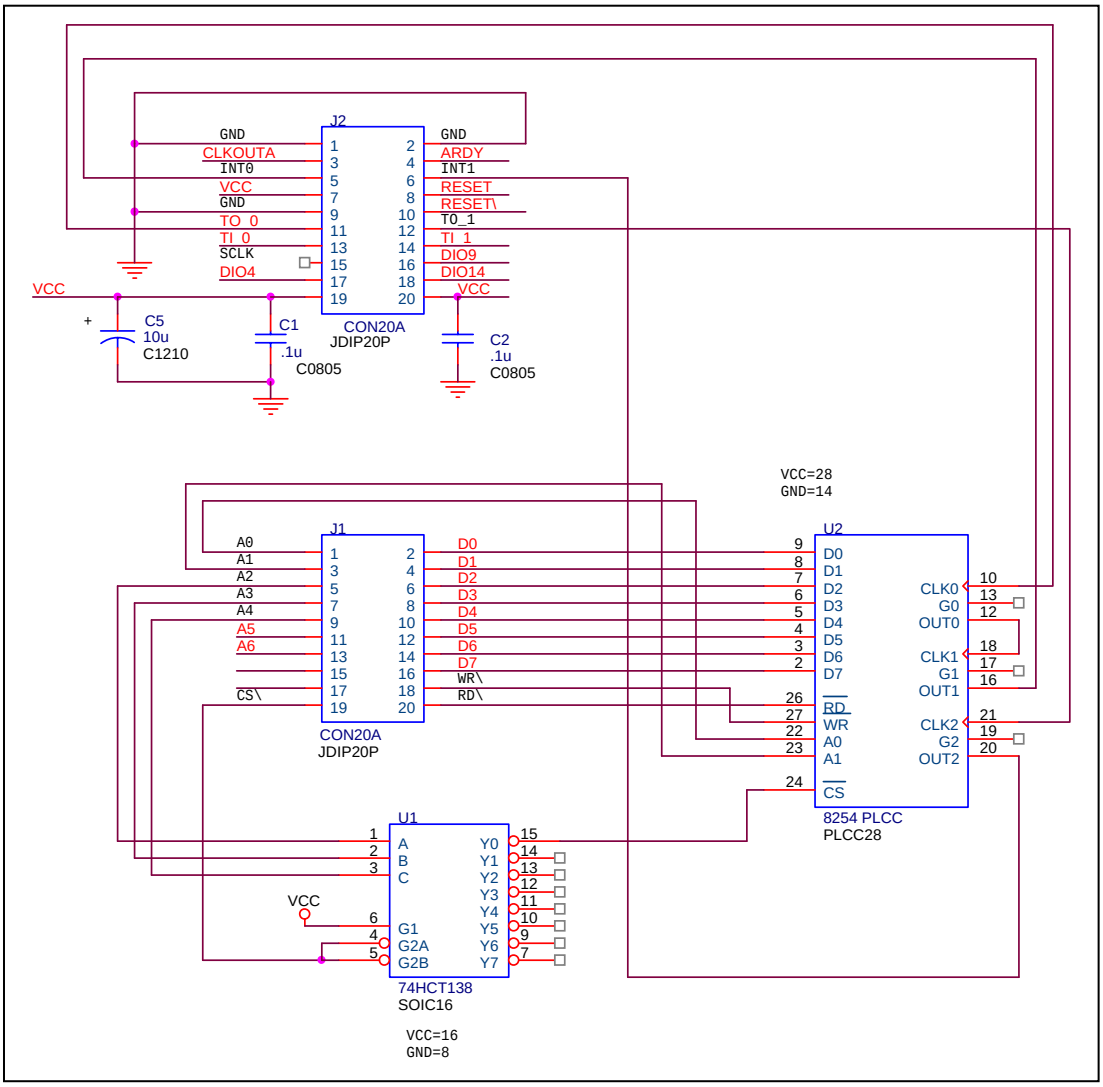
Write value_1 to DO 0 to 7 → outportb (BASE+0, value_1);

Write value_2 to DO 8 to 15 → outportb (BASE+1, value_2);

The power-up default value of BASE is 0.

It is **not** recommended to change the value of BASE from 0 to another value.

2.2.4 8254 & interrupt



The addressing space of 8254 is from BASE+0 to BASE+3 as follows:

Timer/Counter_0 → BASE+0

Timer/Counter_1 → BASE+1

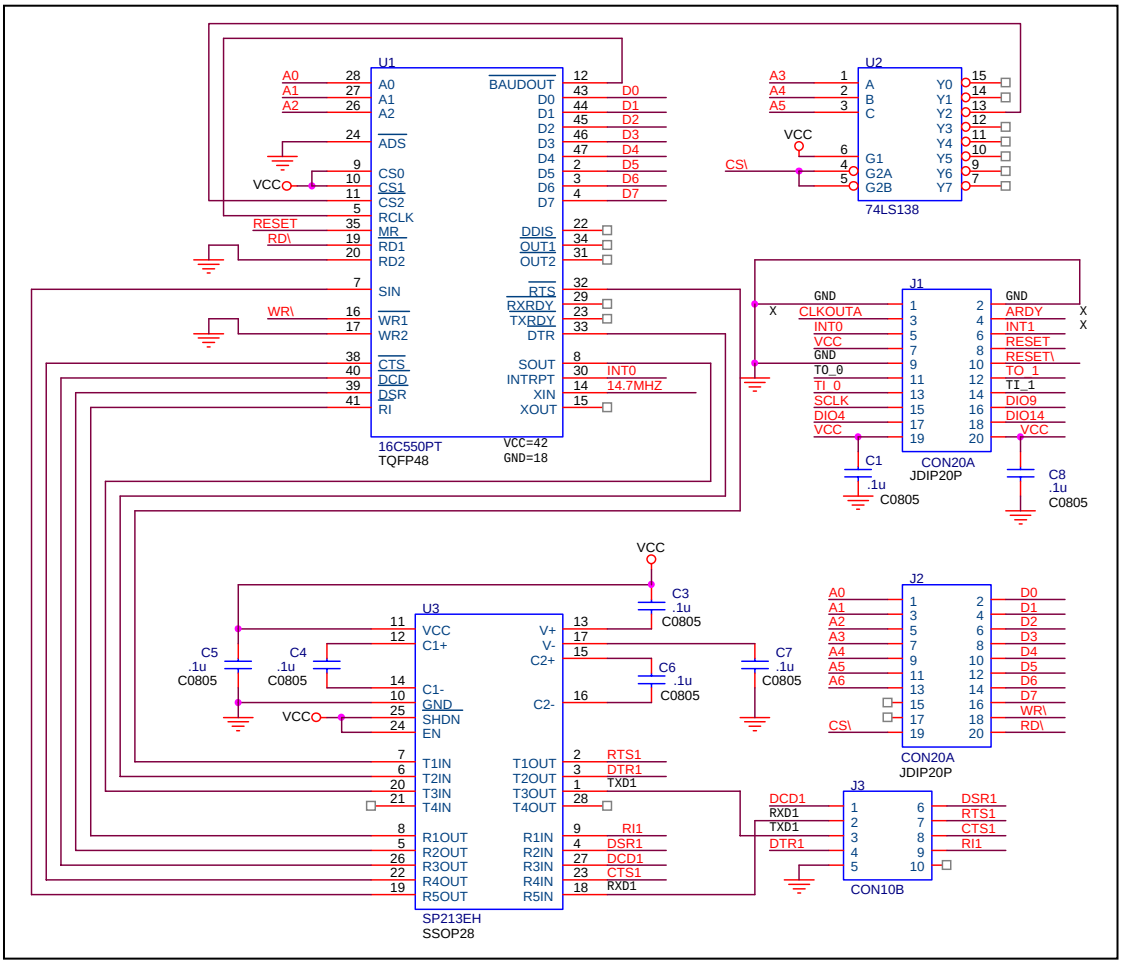
Timer/Counter_2 → BASE+2

Control word → BASE+3

The power-up default value of BASE is 0.

It is **not** recommended to change the value of BASE from 0 to another value.

2.2.5 16550 & interrupt



The addressing space of 16550 is from BASE+0x10 to BASE+0x17 as follows:

```
Txbuf=BASE+0x10          /* tx buffer                          */
Rxbuf=BASE+0x10          /* rx buffer                          */
Dll=BASE+0x10            /* baud lsb                           */
Dlh=BASE+0x11            /* baud msb                           */
Ier=BASE+0x11            /* int enable register                */
Fcr=BASE+0x12            /* FIFO control register                 */
Iir=BASE+0x12            /* Interrupt Identification Register     */
Lcr=BASE+0x13            /* line control register              */
Dfr=BASE+0x13            /* Data format register                  */
Mcr=BASE+0x14            /* modem control register             */
Lsr=BASE+0x15            /* line status register               */
Msr=BASE+0x16            /* modem status register              */
Scr=BASE+0x17            /* Scratch register                      */
```

The power-up default value of BASE is 0.

It is **not** recommended to change the value of BASE from 0 to another value.

Note: it is compatible to **COM3** of 7188XC/7188XB/7188E library.

2.3 Serial Bus

Pin	Name	Default	D/I/O mode	Normal mode
J1.11	TO_0	D/I	I/O_10	Timer output channel_0
J1.12	TO_1	D/I	I/O_1	Timer output channel_1
J1.13	TI_0	D/I	I/O_11	Timer input channel_0
J1.14	TI_1	D/I	I/O_0	Timer input channel_1
J1.15	SCLK	D/O	I/O_26	UZI, don't change to this mode
J1.16	DIO9	D/I	I/O_9	A19, don't change to this mode
J1.17	DIO4	D/I	I/O_4	DT/R, don't change to this mode
J1.18	DIO14	D/I	I/O_14	MCS0, don't change to this mode

Every pin can be configured by mode control register & direction control register as follows:

Mode control register=0xff70	**Direction control register=0xff72**	Programmable Function
0	0	Normal mode
0	1	D/I with pull-up/pull-down resistor (10K)
1	0	D/O
1	1	D/I without pull-up/pull-down register (10K)

After the I/O pins are configured, user can read /write to **data register, 0xff74**, to access these I/O pins. Refer to Sec. 2.3.1 or Sec. 2.3.2 for demo program.

2.3.1 Using the D/I/O 4

```
SetDio4Dir(int dir)     /* select D/I or D/O first */
{
  if(dir){ /* set to input */
     outport(0xff70,inport(0xff70)&(~(1<<4)));/* set MODE to 0 */
     outport(0xff72,inport(0xff72)|(1<<4));          /* set DIR  to 1 */
  }
  else {   /* set to output */
     outport(0xff70,inport(0xff70)|(1<<4));          /* set MODE to 1 */
     outport(0xff72,inport(0xff72)&(~(1<<4)));/* set DIR  to 0 */
  }
}
OutDio4(int data)       /* set the D/O_4 ON or OFF */
{
  if(data)    /* set D/O_4 ON */
     outport(0xFF74,inport(0xFF74)|(1<<4));
  else        /* set D/O_4 OFF */
     outport(0xFF74,inport(0xFF74)&~(1<<4));
}
GetDio4(void)                 /* read the status of D/I_4 */
{
   return inport(0xFF74)&0x0010;}
```

2.3.2 Using the D/I/O 14

```
SetDio14Dir(int dir)    /* select D/I or D/O first */
{
  if(dir){ /* set to input */
     outport(0xff70,inport(0xff70)&(~(1<<14)));       /* set MODE to 0 */
     outport(0xff72,inport(0xff72)|(1<<14));     /* set DIR  to 1 */
  }
  else {   /* set to output */
     outport(0xff70,inport(0xff70)|(1<<14));     /* set MODE to 1 */
     outport(0xff72,inport(0xff72)&(~(1<<14)));       /* set DIR  to 0 */
  }
}
```

```
OutDio14(int data)     /* set the D/O_14 ON or OFF */
{
  if(data)    /* set D/O_14 ON */
     outport(0xFF74,inport(0xFF74)|(1<<14));
  else        /* set D/O_14 OFF */
     outport(0xFF74,inport(0xFF74)&~(1<<14));
}
```

```
GetDio4(void)                  /* read the status of D/I_14 */
{
   return inport(0xFF74)&0x4000;
}
```

2.3.3 Using the SCLK

The 7188 series use this signal as a CLOCK source to drive all on-board serial devices, so it is always be programmed as D/O. Change this signal to other configuration will cause serious errors. User can use this signal to drive external serial devices without any side effects. The software driver provides two subroutine to set SCLK high or low as follows:

```
ClockLow();       /* SCLK=0=Low  */
ClockHigh();      /* SCLK=1=High */
```

3. I/O Expansion Boards

I/O expansion board for prototype & test:

No.	Descriptions	Processor board
X000	Prototype board 1 (64mm * 32mm)	7188XC
X001	Prototype board 2 (64mm * 70mm)	7188XC
X002	Prototype board 3 (114mm * 170mm)	7188XA/XB/XC/EX
X003	Test board for 7188XC &7521	7188XC
X004	Test board for 7188XB & 7188EX	7188XB / EX
X005	Prototype board 4 (38mm * 64mm)	7188XB / EX
X006	Prototype board 5 (72mm * 65mm)	7188XB / EX
I/O expansion board for D/I, D/O or D/I/O:		
X100	8 channels of D/I, 3.5V~30V	7188XC
X101	8 channels of D/O, TTL (64mA)	7188XC
X102	2 channels of relay output	7188XC
X103	5 channels of isolated D/I (3.5V ~ 30V)	7188XC
X104	8 channels of D/I/O (single channel programmable)	7188XC
X105	8 channels of D/I/O (8-channels programmable)	7188XC
X106	Extra 2 channels of DO or 3 channels of D/I	7188XC
X107	6 channels of D/I + 7 channels of D/O	7188XB / EX
I/O expansion board for A/D:		
X200	1 channel of 12-bit A/D (0 ~ 2.5V)	7188XC
I/O expansion board for D/A:		
X300	2 channels of 12-bit D/A (4.095V,drive=5mA, sink=0.5mA)	7188XC
X301	1 channel of A/D + 1 channel of D/A	7188XC
I/O expansion board for Timer/Counter:		
X400	3 channels of 16-bit timer/counter (8254)	7188XC
I/O expansion board for RS-232:		
X500	1 channel of RS-232, modem control, 115.2K max. (RI, DSR, DCD, RTS, CTS, TXD, RXD, GND)	7188XC
X501	1 channels of RS-232 (for 7522), (RTS, CTS, TXD, RXD, GND)	7188XC
X502	2 channel of RS-232 (for 7523), COM4 (TXD, RXD,GND) COM3 (RTS, CTS, TXD, RXD, GND)	7188XC
X503	1 channel of RS-232, (RTS, CTS, TXD, RXD,GND)	7188XB / EX

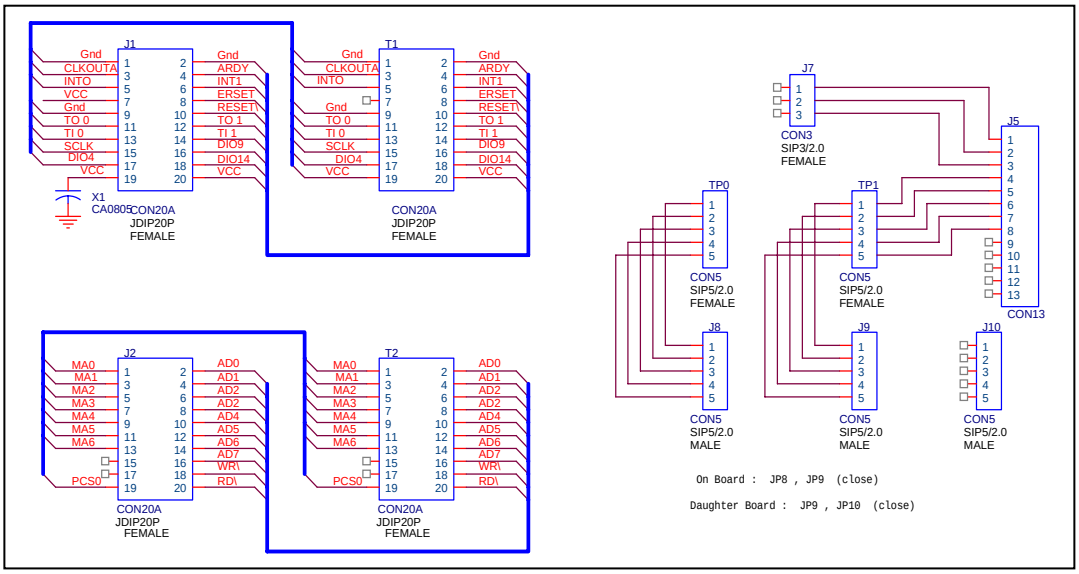
No.	Descriptions	Processor board
X504	2 channel of RS-232, COM3 (RTS, CTS, TXD, RXD) COM4 (RI, DSR, DCD, RTS, CTS, TXD, RXD, DTR)	7188XB / EX

I/O expansion board for storage devices:

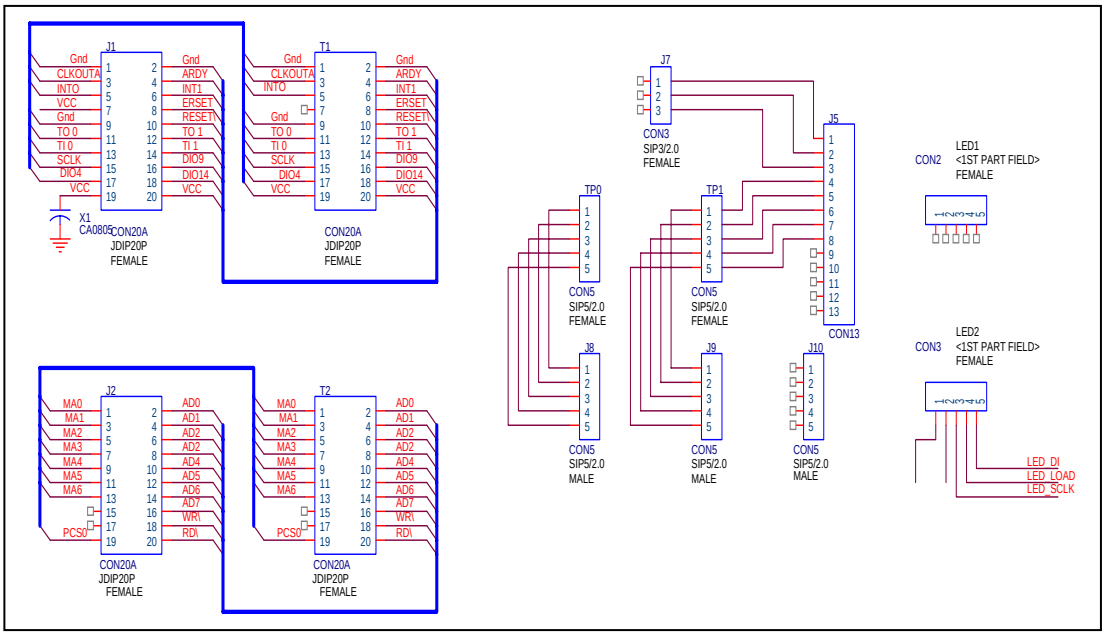
X600	4M bytes NAND Flash	7188XA/XB/XC/EX
X601	8M bytes NAND Flash	7188XA/XB/XC/EX
X602	16M bytes NAND Flash	7188XA/XB/XC/EX
X603	32M bytes NAND Flash	7188XA/XB/XC/EX
X607	128K battery backup SRAM	7188XA/XB/XC/EX

X000/001/002: Prototype Board

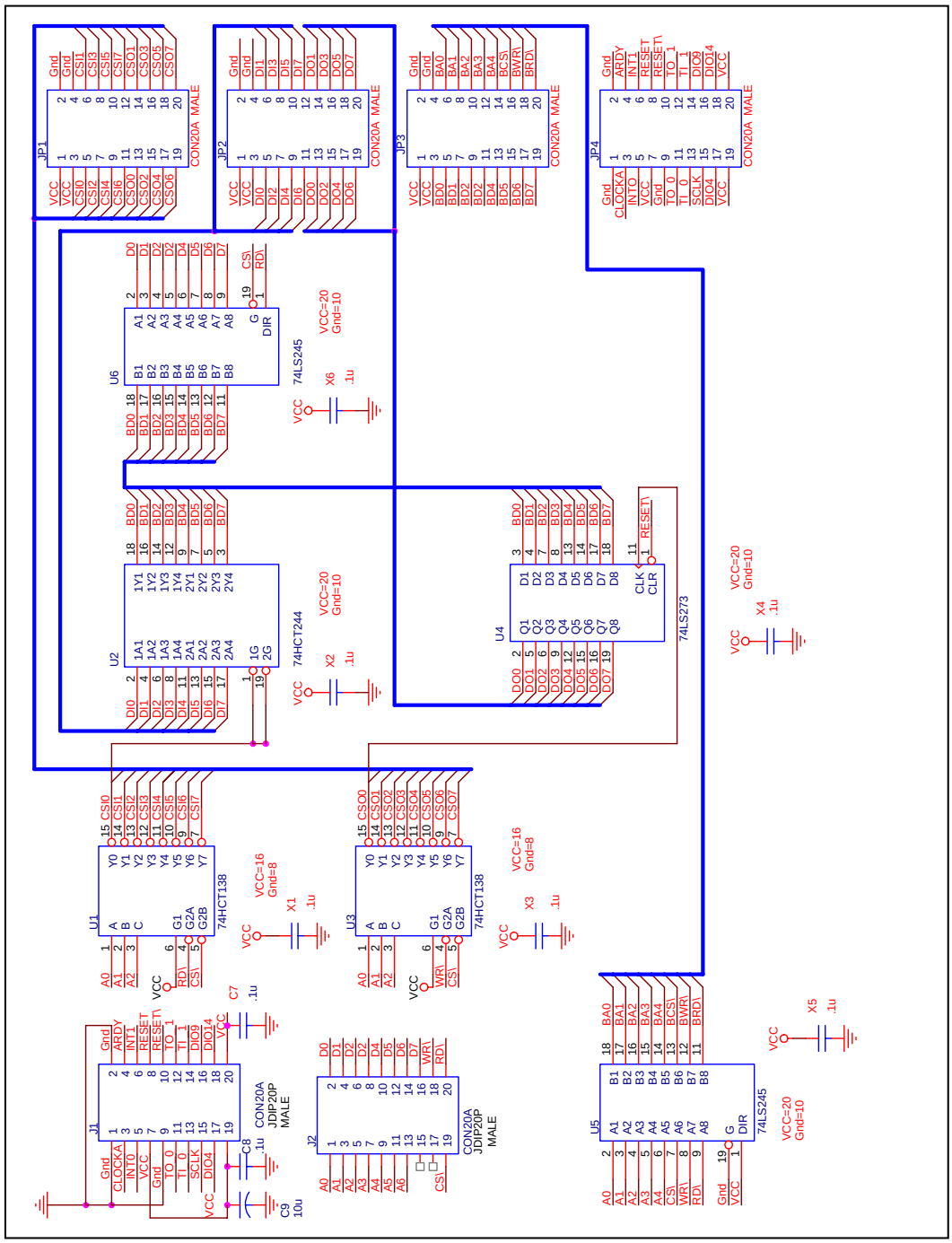
X000: 65mm * 35mm



X001: 65mm * 70mm

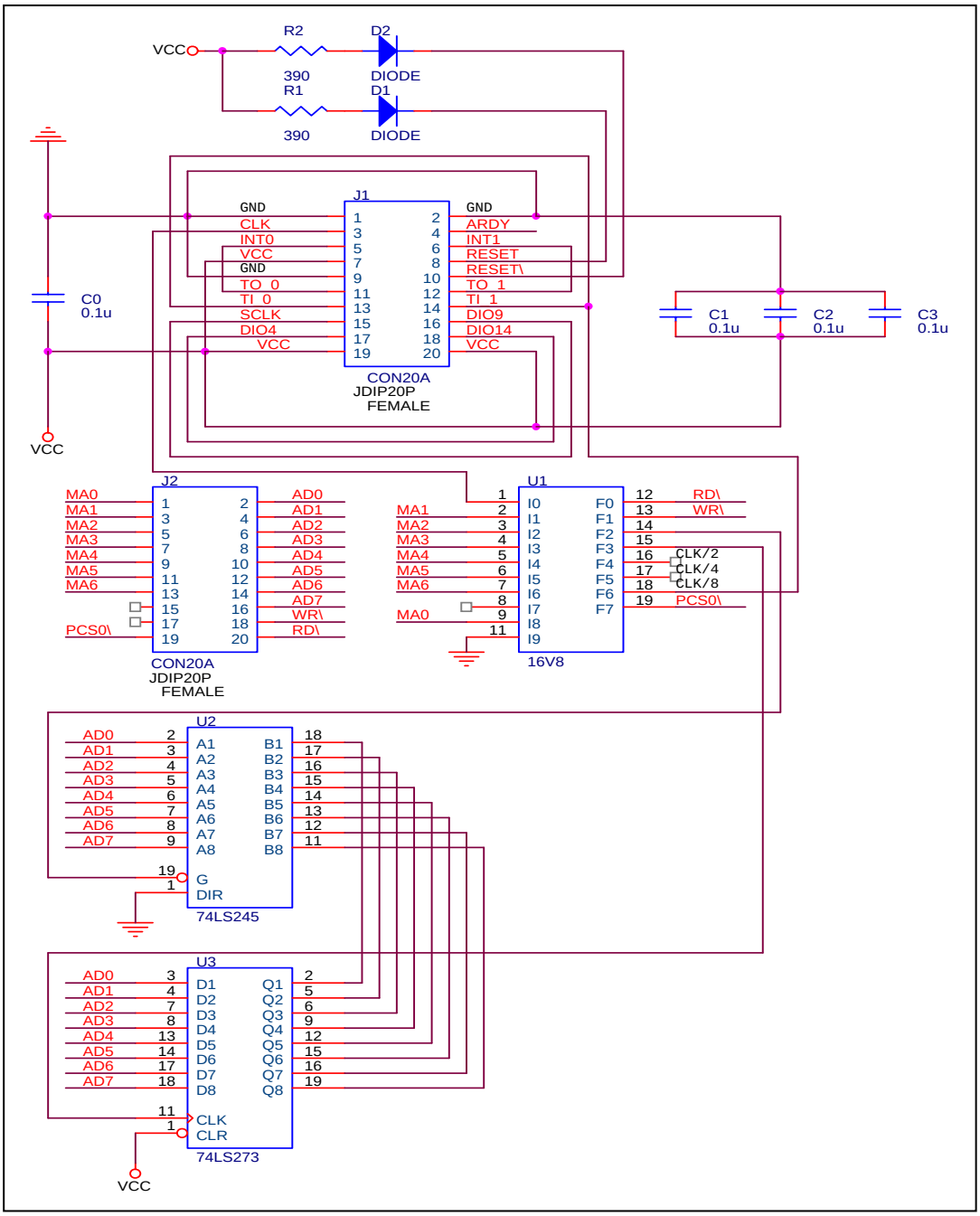


X002: 115mm * 170mm



3.1 X003: Test Board 1

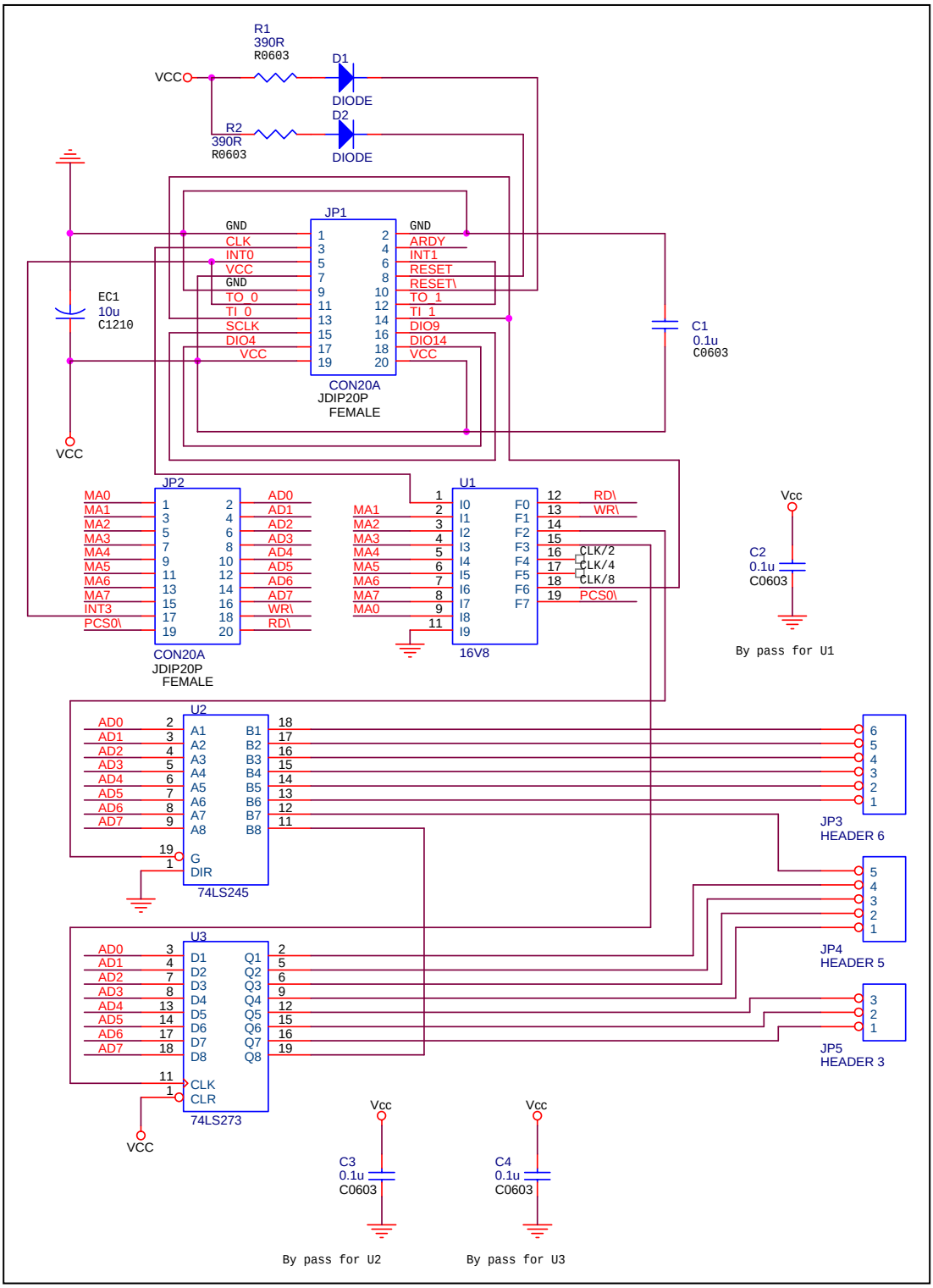
- For 7188XC & 7521
- Refer to C:\7188xc\demo\ioexpbus\X003*.* for demo program



```
;PALASM Design Description

;---------------------------------- Declaration Segment ------------
TITLE        X003
PATTERN  P. F. Huang
REVISION 1.0
AUTHOR   P. F. Huang
COMPANY  ICP DAS
DATE         April/02/2000

CHIP  _X003  PALCE16V8H

;---------------------------------- PIN Declarations ---------------
PIN  1            CLK                        COMBINATORIAL ;
PIN  2            A1                         COMBINATORIAL ;
PIN  3            A2                         COMBINATORIAL ;
PIN  4            A3                         COMBINATORIAL ;
PIN  5            A4                         COMBINATORIAL ;
PIN  6            A5                         COMBINATORIAL ;
PIN  7            A6                         COMBINATORIAL ;
;IN  8        A7                         COMBINATORIAL ;
PIN  9            A0                         COMBINATORIAL ;

PIN  19     CS1                        COMBINATORIAL ;
PIN  12     WR                         COMBINATORIAL ;
PIN  13     RD                         COMBINATORIAL ;
PIN  14     DI1                        COMBINATORIAL ;
PIN  15     DO1                        COMBINATORIAL ;

PIN  16     Q0                         REGISTERED ;
PIN  17     Q1                         REGISTERED ;
PIN  18     Q2                         REGISTERED ;


;---------------------------------- Boolean Equation Segment ------
EQUATIONS

/DI1   =  /CS1*/A6*/A5*/A4*/A3*/A2*/A1*/A0*/RD;
/DO1   =  /CS1* A6* A5* A4* A3* A2* A1* A0*/WR;

Q0     = /Q0;
Q1     = Q0 * /Q1 + /Q0 * Q1;
Q2     = Q0*Q1*/Q2 + /Q0*/Q1*Q2 + Q0*/Q1*Q2 + /Q0*Q1*Q2;


;PIN 11  = connect to GND
;DI1        = inportb(0)
;DO1        = outportb(0xff)
;Q0         = CLK/2
;Q1         = CLK/4;
;Q3         = CLK/8;
```

3.2 X004: Test Board 2

- For 7188XB & 7188E series
- Refer to C:\7188xc\demo\ioexpbus\X004*.* for demo program



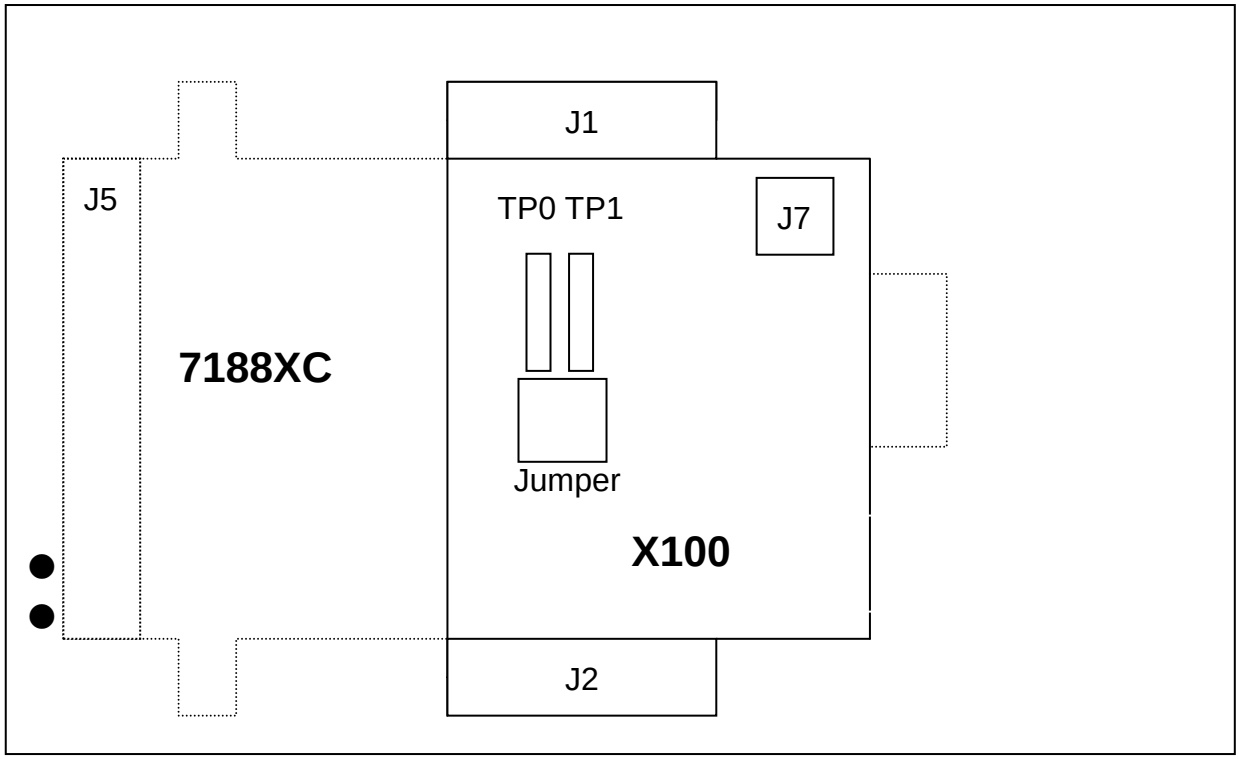
```
;PALASM Design Description

;---------------------------------- Declaration Segment ------------
TITLE        X004
PATTERN  P. F. Huang
REVISION 1.0
AUTHOR   P. F. Huang
COMPANY  ICP DAS
DATE         April/02/2000

CHIP  _X004  PALCE16V8H

;---------------------------------- PIN Declarations ---------------
PIN  1          CLK                     COMBINATORIAL ;
PIN  2          A1                      COMBINATORIAL ;
PIN  3          A2                      COMBINATORIAL ;
PIN  4          A3                      COMBINATORIAL ;
PIN  5          A4                      COMBINATORIAL ;
PIN  6          A5                      COMBINATORIAL ;
PIN  7          A6                      COMBINATORIAL ;
PIN  8          A7                      COMBINATORIAL ;
PIN  9          A0                      COMBINATORIAL ;

PIN  19    CS1                  COMBINATORIAL ;
PIN  12    WR                   COMBINATORIAL ;
PIN  13    RD                   COMBINATORIAL ;
PIN  14    DI1                  COMBINATORIAL ;
PIN  15    DO1                  COMBINATORIAL ;

PIN  16    Q0                   REGISTERED ;
PIN  17    Q1                   REGISTERED ;
PIN  18    Q2                   REGISTERED ;


;---------------------------------- Boolean Equation Segment ------
EQUATIONS

/DI1   =  /CS1*/A7*/A6*/A5*/A4*/A3*/A2*/A1*/A0*/RD;
/DO1   =  /CS1* A7* A6* A5* A4* A3* A2* A1* A0*/WR;

Q0     = /Q0;
Q1     = Q0 * /Q1 + /Q0 * Q1;
Q2     = Q0*Q1*/Q2 + /Q0*/Q1*Q2 + Q0*/Q1*Q2 + /Q0*Q1*Q2;

;PIN 11  = connect to GND
;DI1       = inportb(0)
;DO1       = outportb(0xff)
;Q0        = CLK/2
;Q1        = CLK/4;
;Q3        = CLK/8;
```

3.3 X100: DI * 8

3.3.1 Specifications

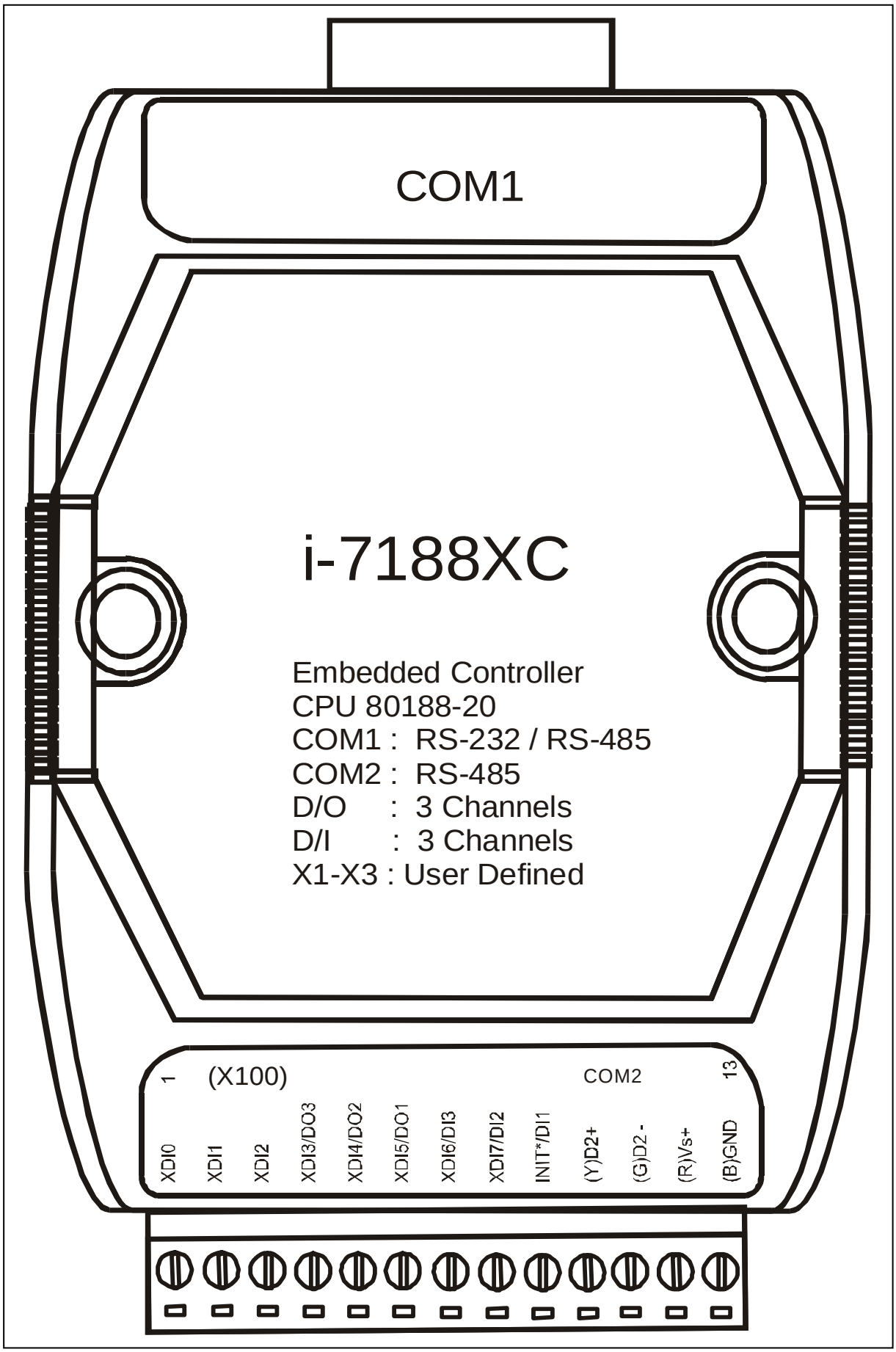
- 8 channels of D/I, Logic high level: (3.5V~30V), Logic low level: (0V~1V)
- For 7188XC series

3.3.2 Pin Assignment & Jumper Setting

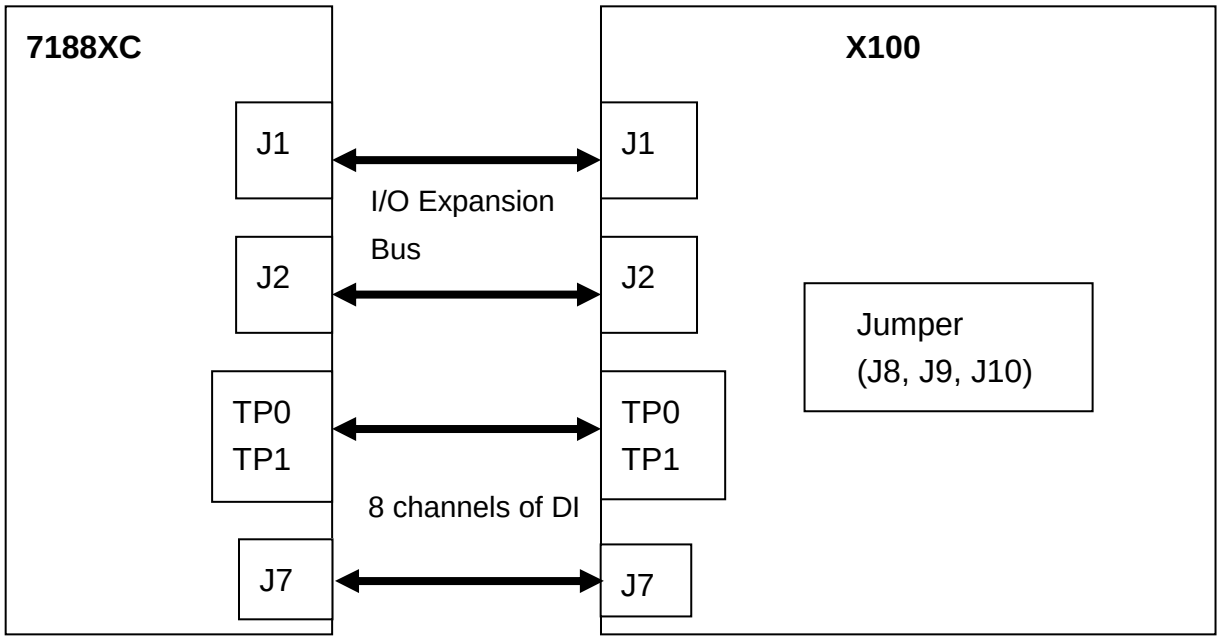


- **Note: user should remove R19, R20, R21, R22 and R23 in the 7188XC first.**
- **J1:** I/O expansion bus, connect to J1 of 7188XC
- **J2:** I/O expansion bus, connect to J2 of 7188XC
- **J7:** Three channels of 8 DI
- **TP0:** Original function on 7188XC
- **TP1:** Five channels of 8 DI
- **Jumper:** Select **TP0** or **TP1** function
  - **TP0:** J9 and J8 closed
  - **TP1:** J9 and J10 closed
- **J5:**. The pin assignment of J5 is given as following: (the pin assignment will be different based on different jumper setting)

XDI4 initial state must be High. If its initial state is LOW, system clock will be reduced to 10M. So all clock-related libraries will be only half-speed.


COM1
i-7188XC
Embedded Controller
CPU 80188-20
COM1 : RS-232 / RS-485
COM2 : RS-485
D/O : 3 Channels
D/I : 3 Channels
X1-X3 : User Defined
1
(X100)
COM2
13
XDI0
XDI1
XDI2
XDI3/DO3
XDI4/DO2
XDI5/DO1
XDI6/DI3
XDI7/DI2
INIT*/DI1
(Y)D2+
(G)D2-
(R)Vs+
(B)GND

3.3.3 Block Diagram



3.3.4 Programming

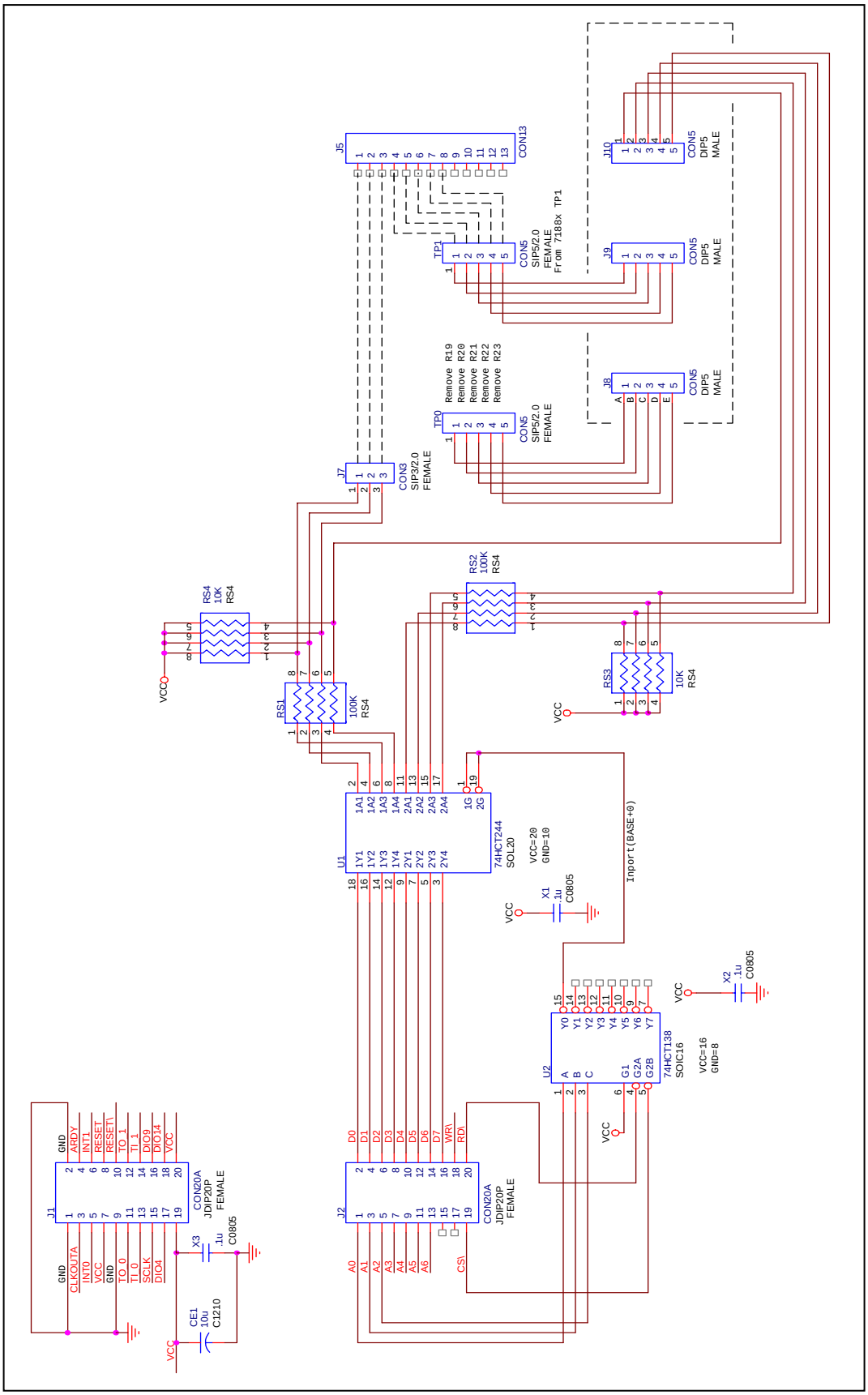
DiVal = **inportb(BASE); /* for all 8-channels */**

Note: 1. The default value of BASE is 0.

2. It is **not** recommended to change the value of BASE from 0 to another value.

3. DiVal=0 → all 8-channel are Low
   DiVal=1 → Chennel_0 is High, the other channels are Low
   DiVal=0xff → all 8-channel are High

3.3.5 Circuit Diagram

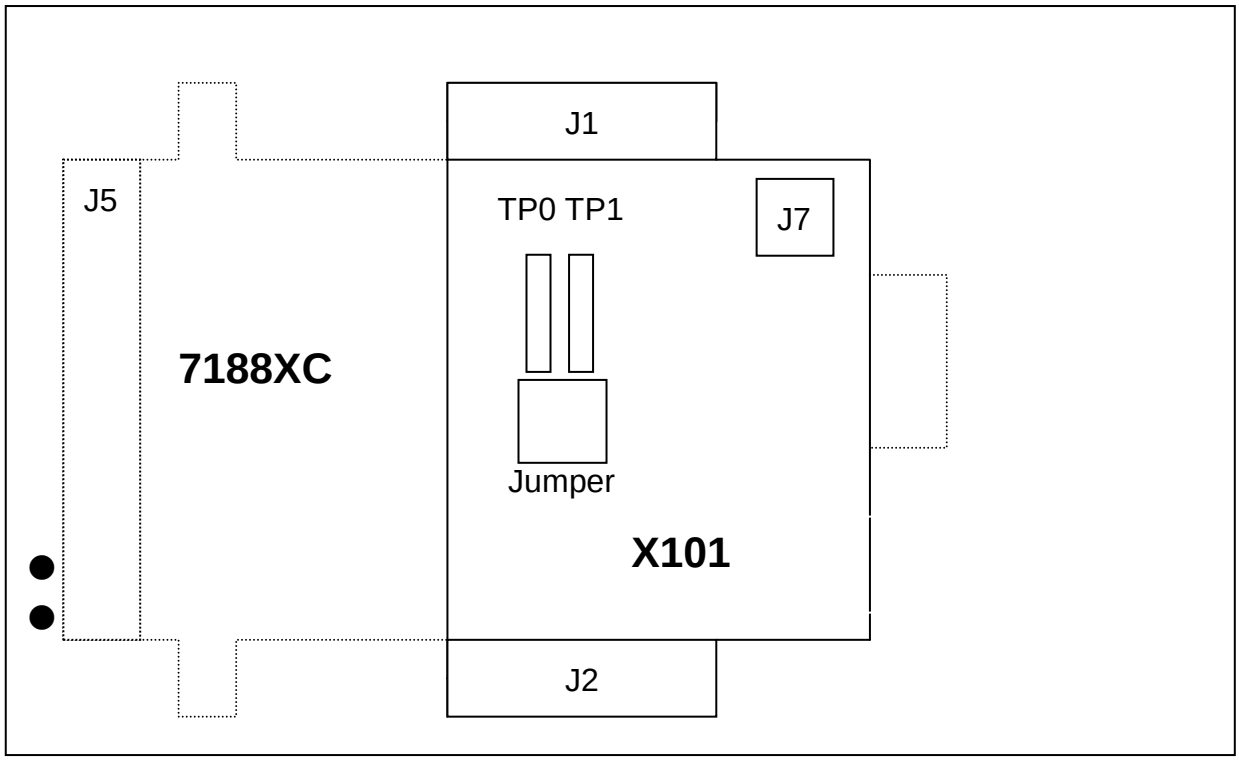


3.4 X101: DO * 8

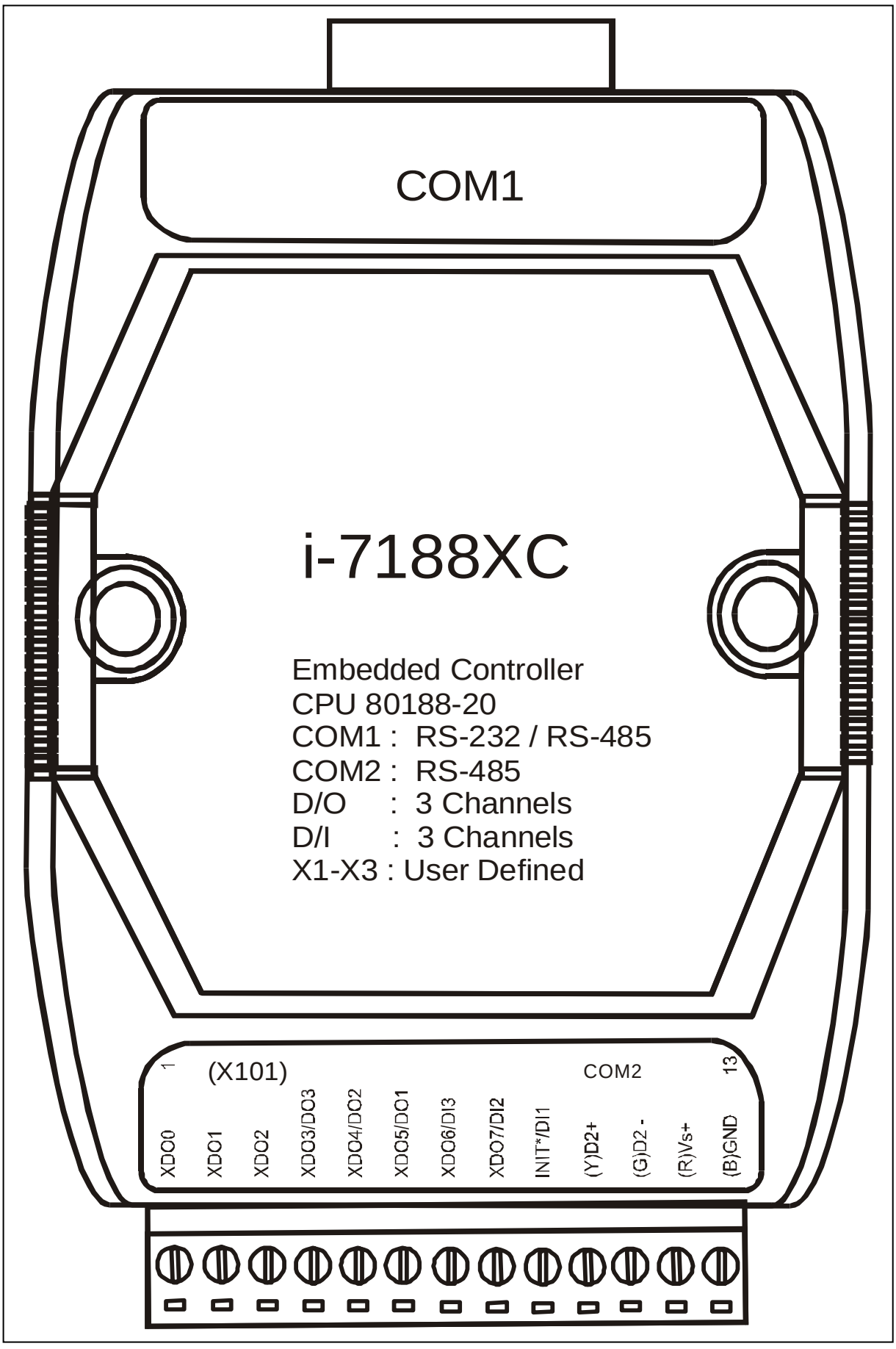
3.4.1 Specifications

- 8 channels of D/O, TTL (Sink current: 64mA)
- For 7188XC series

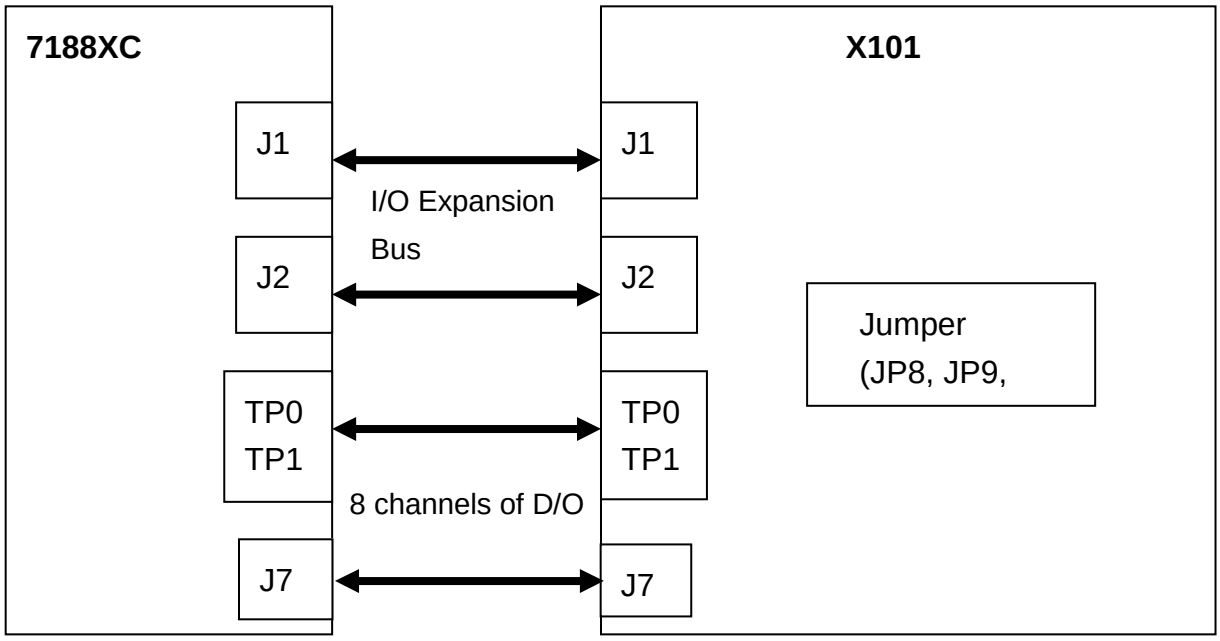
3.4.2 Pin Assignment & Jumper Setting



- **Note: user should remove R19, R20, R21, R22 and R23 in the 7188XC first.**
- **J1:** I/O expansion bus, connect to J1 of 7188XC
- **J2:** I/O expansion bus, connect to J2 of 7188XC
- **J7:** Three channel of 8 D/O
- **TP0:** Original function on 7188XC
- **TP1:** Five channel of 8 D/O
- **Jumper:** Select **TP0** or **TP1** function
  TP0: JP9 and JP8 closed
  TP1: JP9 and JP10 closed
- **J5:**. The pin assignment of J5 is given as following: (the pin assignment will be different based on different jumper setting)


COM1
i-7188XC
Embedded Controller
CPU 80188-20
COM1 : RS-232 / RS-485
COM2 : RS-485
D/O : 3 Channels
D/I : 3 Channels
X1-X3 : User Defined
1
(X101)
COM2
13
XDO0
XDO1
XDO2
XDO3/DO3
XDO4/DO2
XDO5/DO1
XDO6/DI3
XDO7/DI2
INIT*/DI1
(Y)D2+
(G)D2 -
(R)Vs+
(B)GND

3.4.3 Block Diagram



3.4.4 Programming

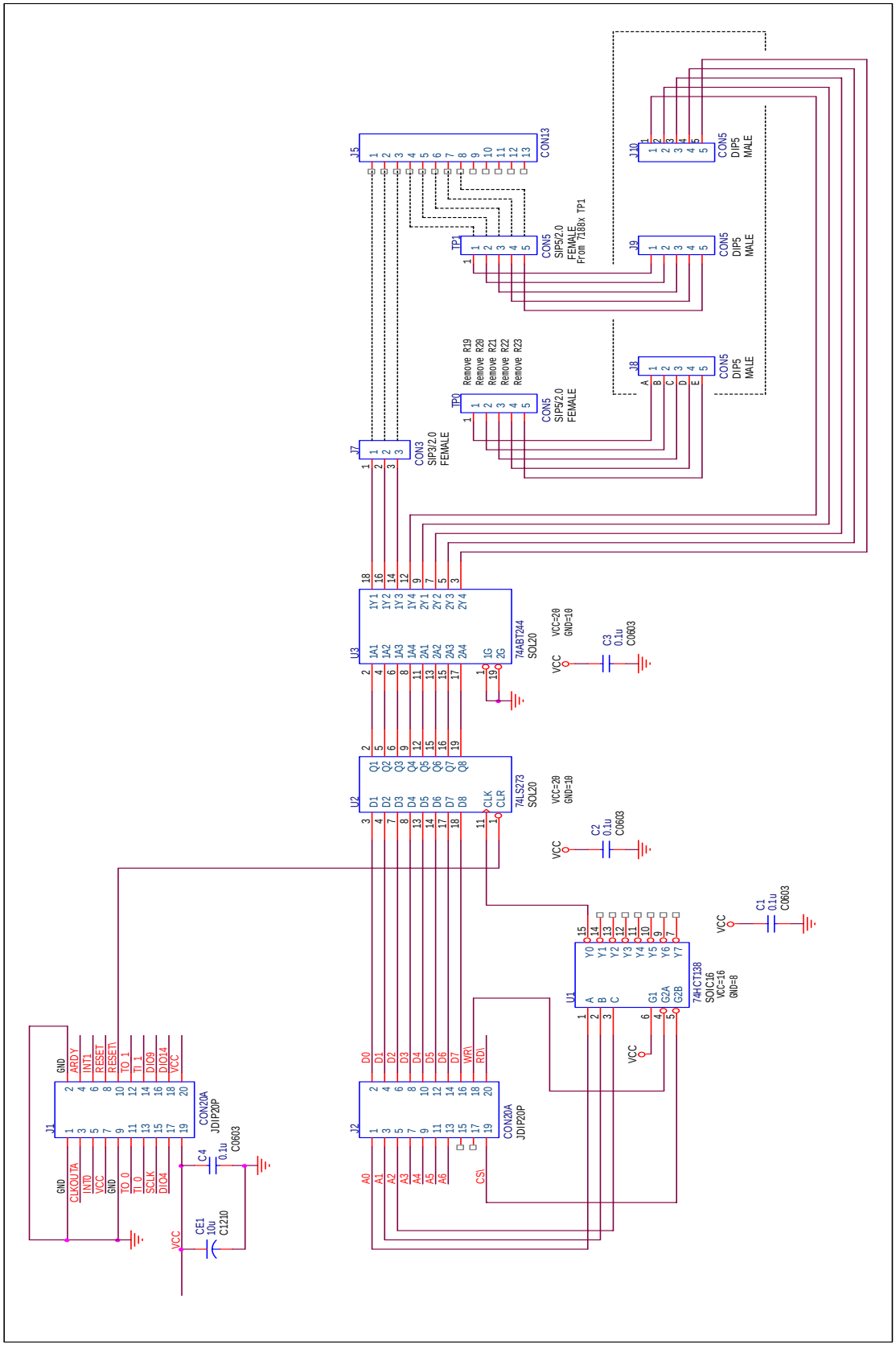
outportb(BASE, DoVal); /* for all 8-channels */

Note: 1. The default value of BASE is 0.

2. It is **not** recommended to change the value of BASE from 0 to another value.

3. DoVal=0 → turn all 8-channel OFF
   DoVal=1 → turn chennel_0 ON, the other channels OFF
   DoVal=0xff→ turn all 8-channel ON

3.4.5 Circuit Diagram

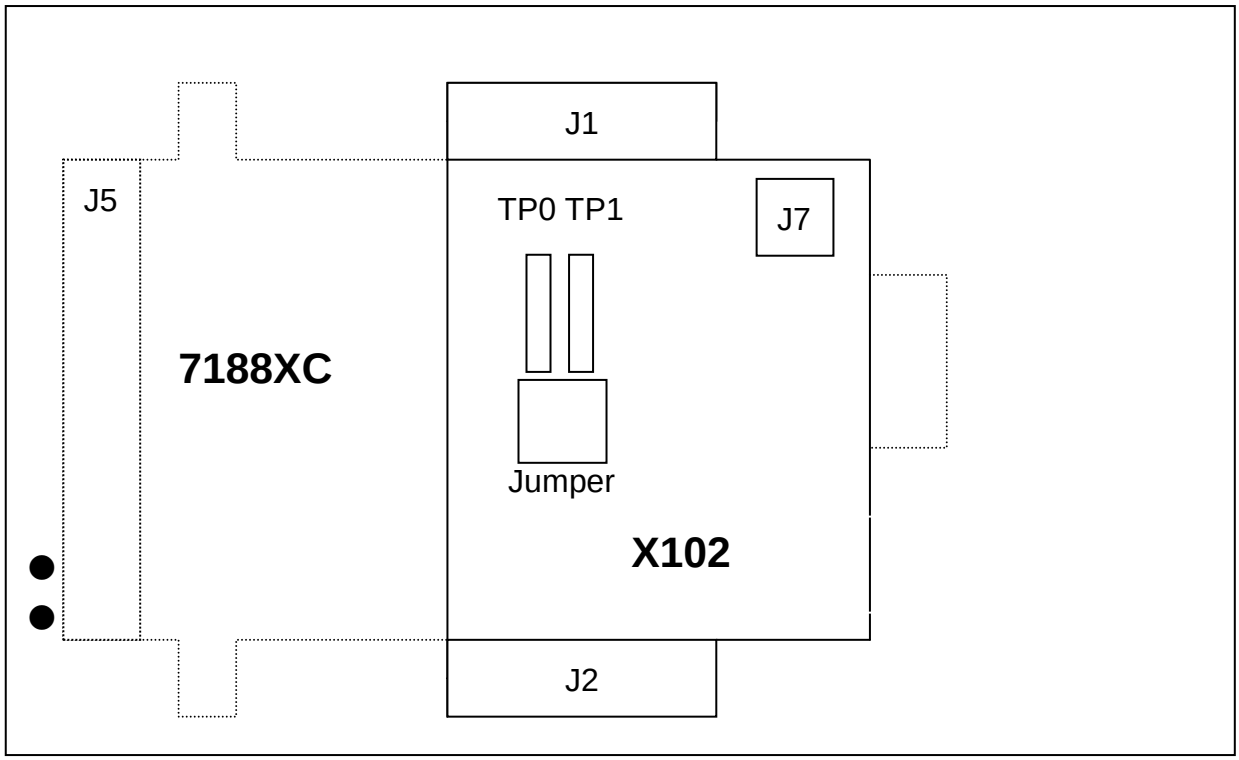


X102: Relay * 2

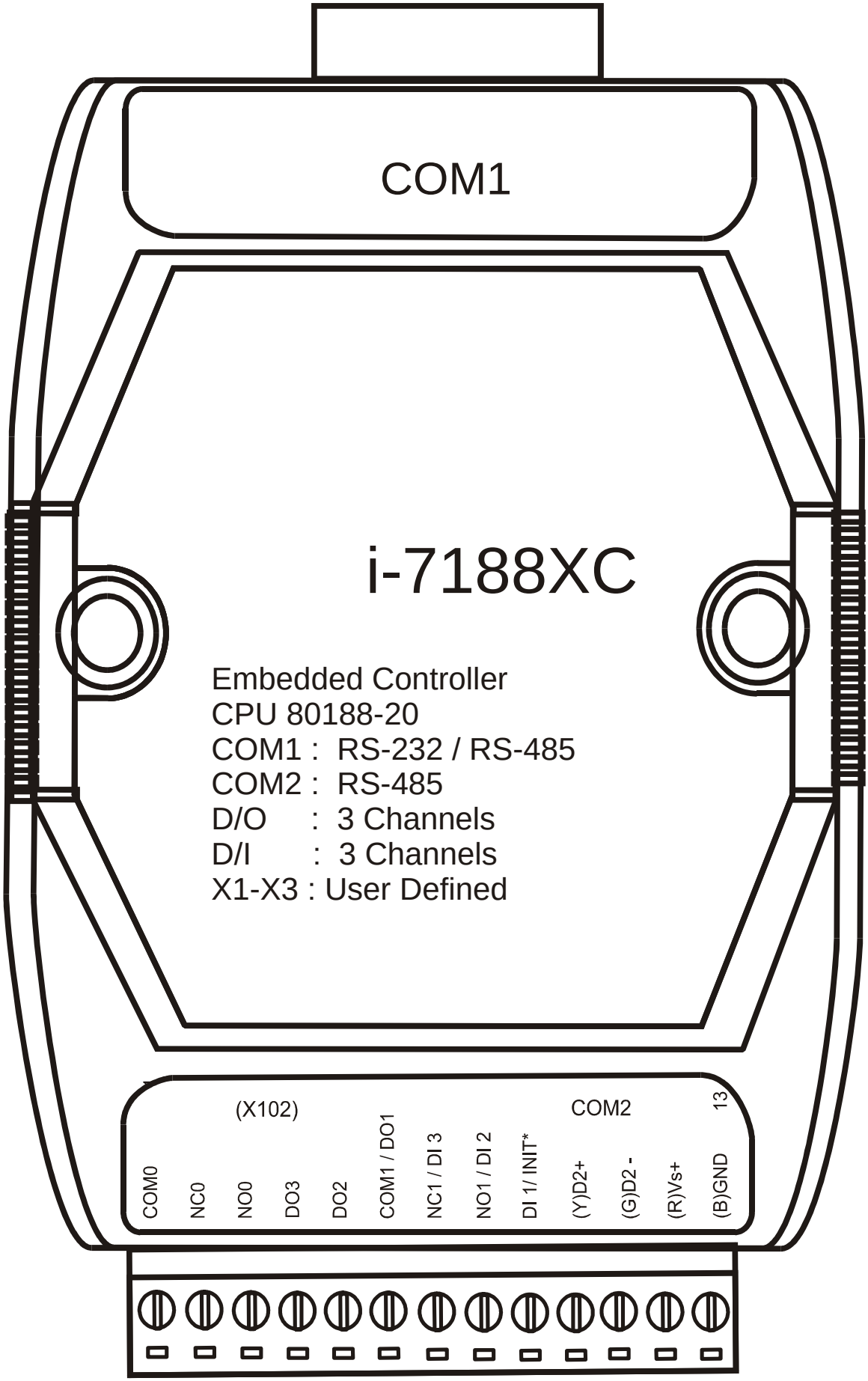
3.4.6 Specifications

- 2 channels of relay output
- For 7188XC series

3.4.7 Pin Assignment & Jumper Setting



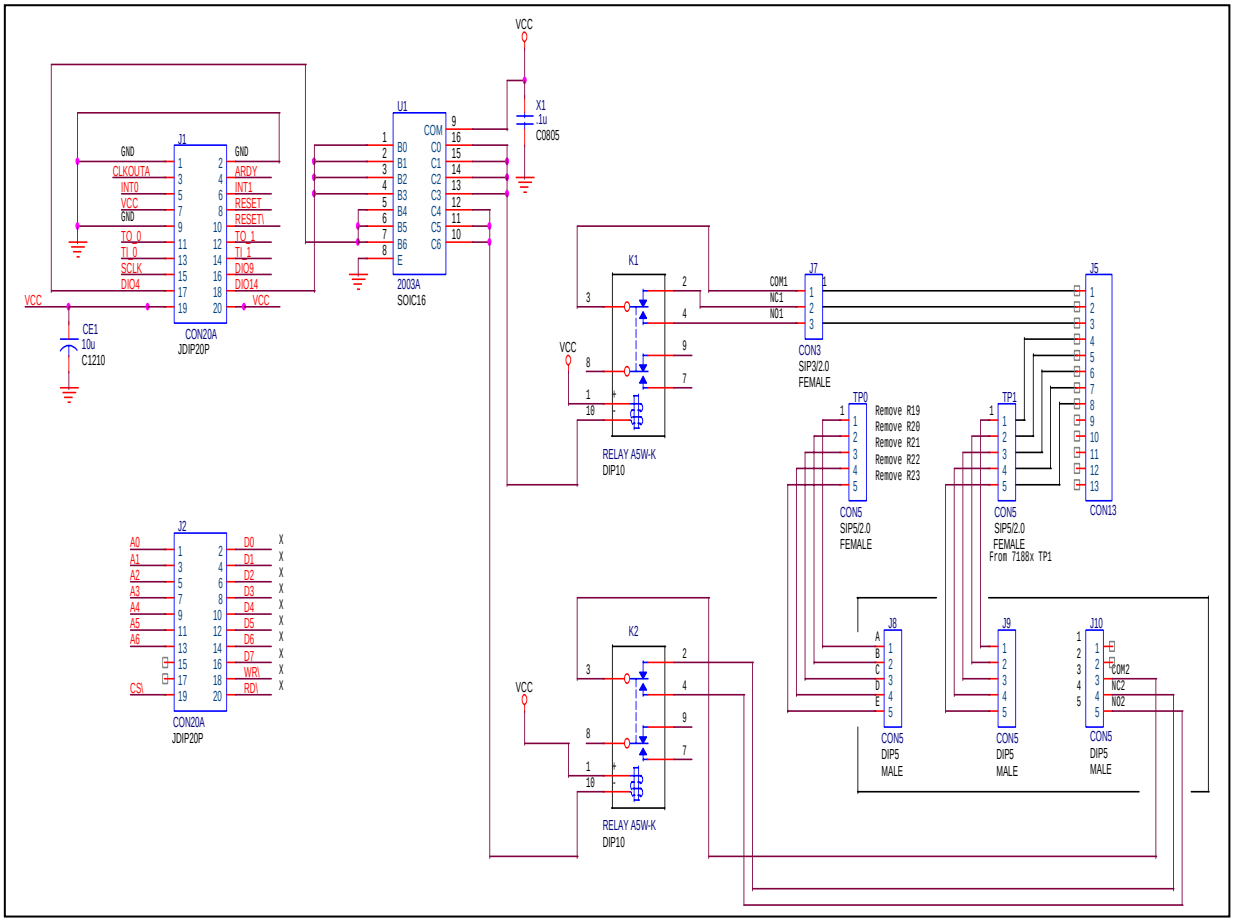
- **Note: user should remove R19, R20, R21, R22 and R23 in the 7188XC first.**
- **J1:** I/O expansion bus, connect to J1 of 7188XC
- **J2:** I/O expansion bus, connect to J2 of 7188XC
- **J7:** One channel of relay output
- **TP0:** Original function on 7188XC
- **TP1:** One channel of relay output
- **Jumper:** Select **TP0** or **TP1** function
  - **TP0:** JP9 and JP8 closed
  - **TP1:** JP9 and JP10 closed
- **J5:** The pin assignment of J5 is given as follows: (the pin assignment will be different based on different jumper setting)


COM1
i-7188XC
Embedded Controller
CPU 80188-20
COM1 : RS-232 / RS-485
COM2 : RS-485
D/O : 3 Channels
D/I : 3 Channels
X1-X3 : User Defined
(X102)
COM2
13
COM0
NC0
NO0
DO3
DO2
COM1 / DO1
NC1 / DI 3
NO1 / DI 2
DI 1 / INIT*
(Y)D2+
(G)D2 -
(R)Vs+
(B)GND

3.4.8 Programming

```
SetDio4Dir( 0 );        // Set channel-0 to DO //
SetDio14Dir( 0 );       // Set channel-1 to DO

SetDio4Low();           // Turn channel_0 relay OFF
SetDio14Low();          // Turn channel_1 relay OFF

SetDio4High();          // Turn channel_0 relay ON
SetDio14High();         // Turn channel_1 relay ON
```

3.4.9 Circuit Diagram

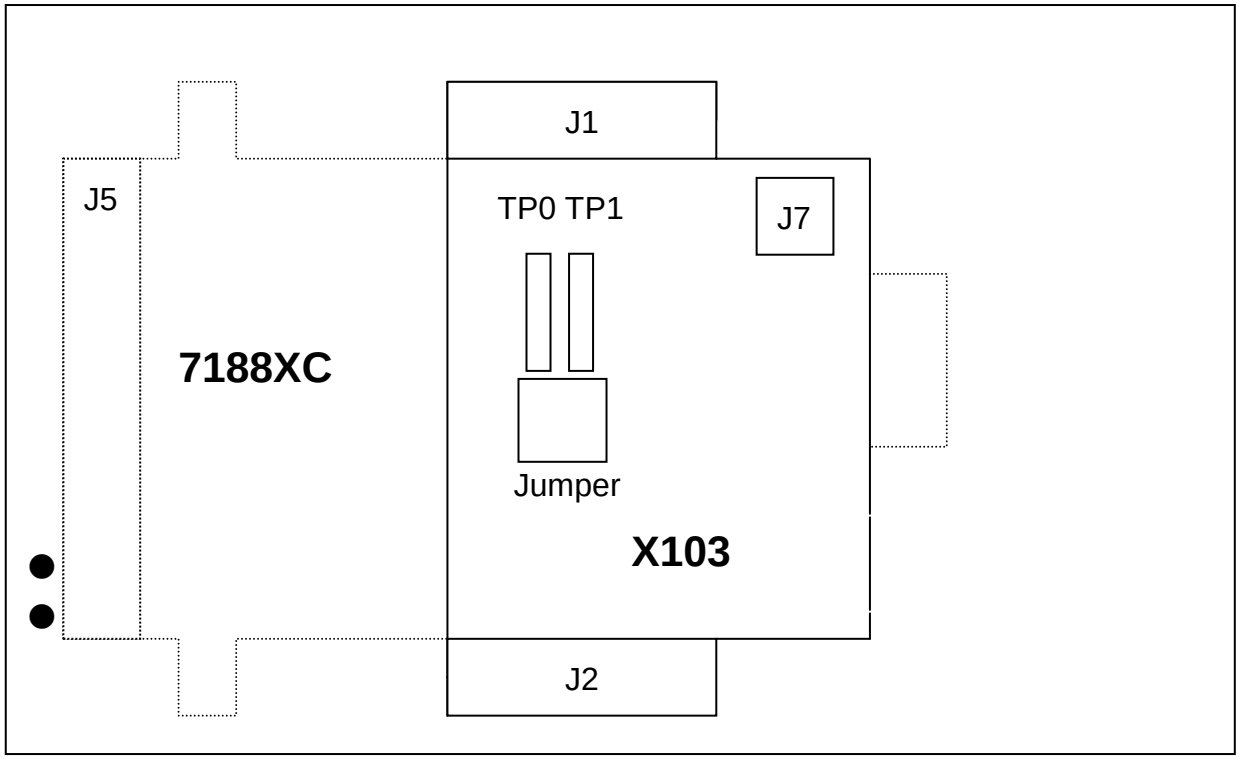


3.5 X103: Isolated DI * 7

3.5.1 Specifications

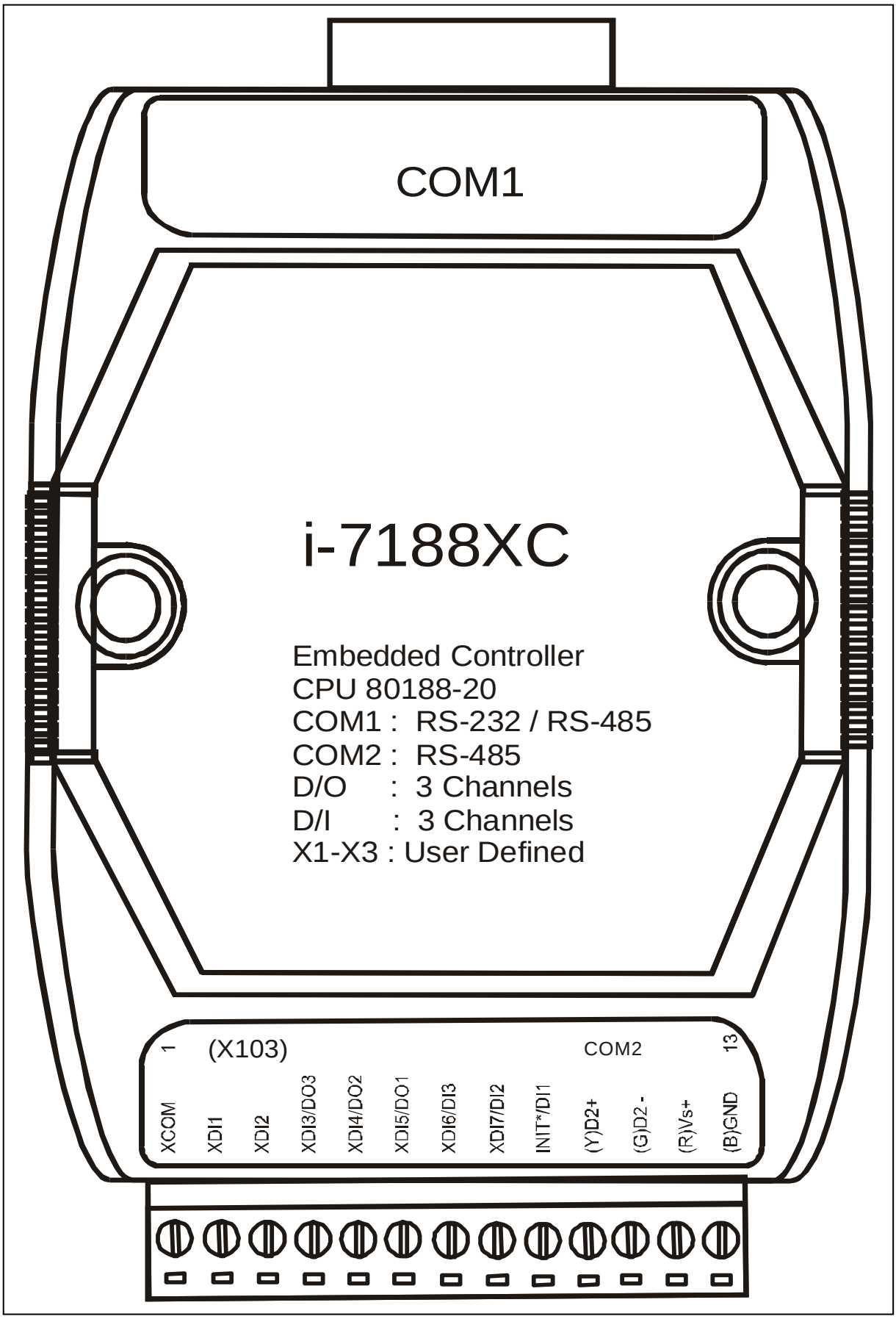
- 7 channels of isolated DI, Logic high level: (3.5V~30V)
- For 7188XC series

3.5.2 Pin Assignment & Jumper Setting

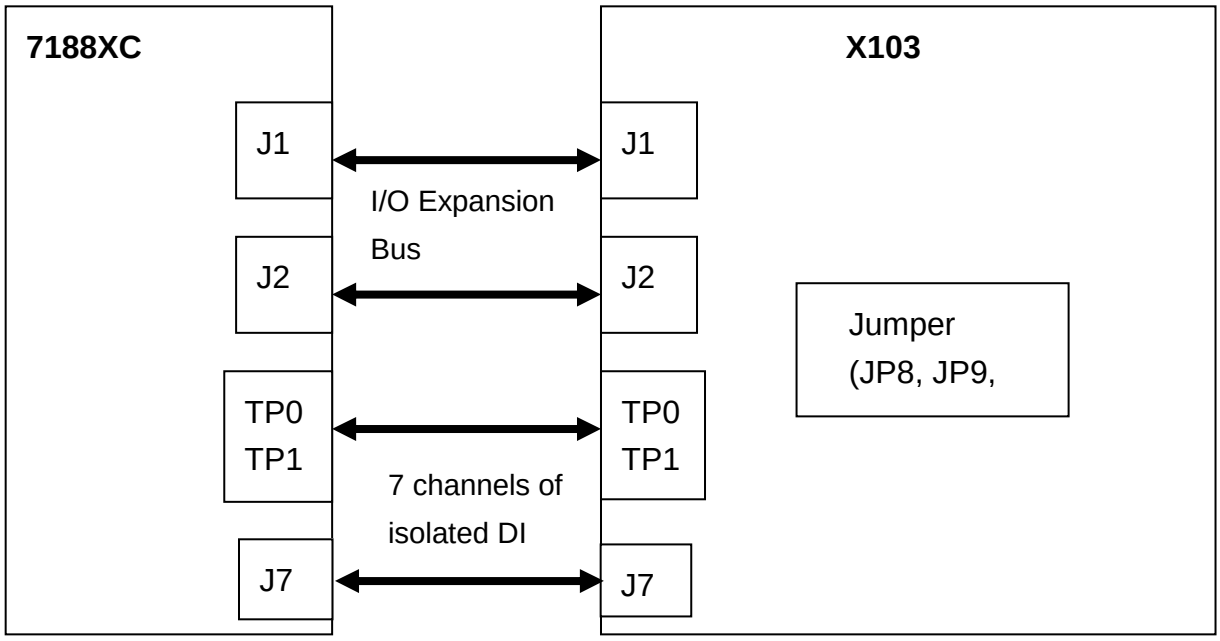


- **Note: user should remove R19, R20, R21, R22, R23 in the 7188XC first.**
- **J1:** I/O expansion bus, connect to J1 of 7188XC
- **J2:** I/O expansion bus, connect to J2 of 7188XC
- **J7:** Two channels of isolated DI
- **TP0:** Original function on 7188XC
- **TP1:** Five channels of isolated DI
- **Jumper:** Select **TP0** or **TP1** function
  TP0: JP9 and JP8 closed
  TP1: JP9 and JP10 closed
- **J5:** The pin assignment of J5 is given as follows: (the pin assignment will be different based on different jumper setting)

XDI4 initial state must be High. If its initial state is LOW, system clock will be reduced to 10M. So all clock-related libraries will be only half-speed.


COM1
i-7188XC
Embedded Controller
CPU 80188-20
COM1 : RS-232 / RS-485
COM2 : RS-485
D/O : 3 Channels
D/I : 3 Channels
X1-X3 : User Defined
1
(X103)
COM2
13
XCOM
XDI1
XDI2
XDI3/DO3
XDI4/DO2
XDI5/DO1
XDI6/DI3
XDI7/DI2
INIT*/DI1
(Y)D2+
(G)D2 -
(R)Vs+
(B)GND

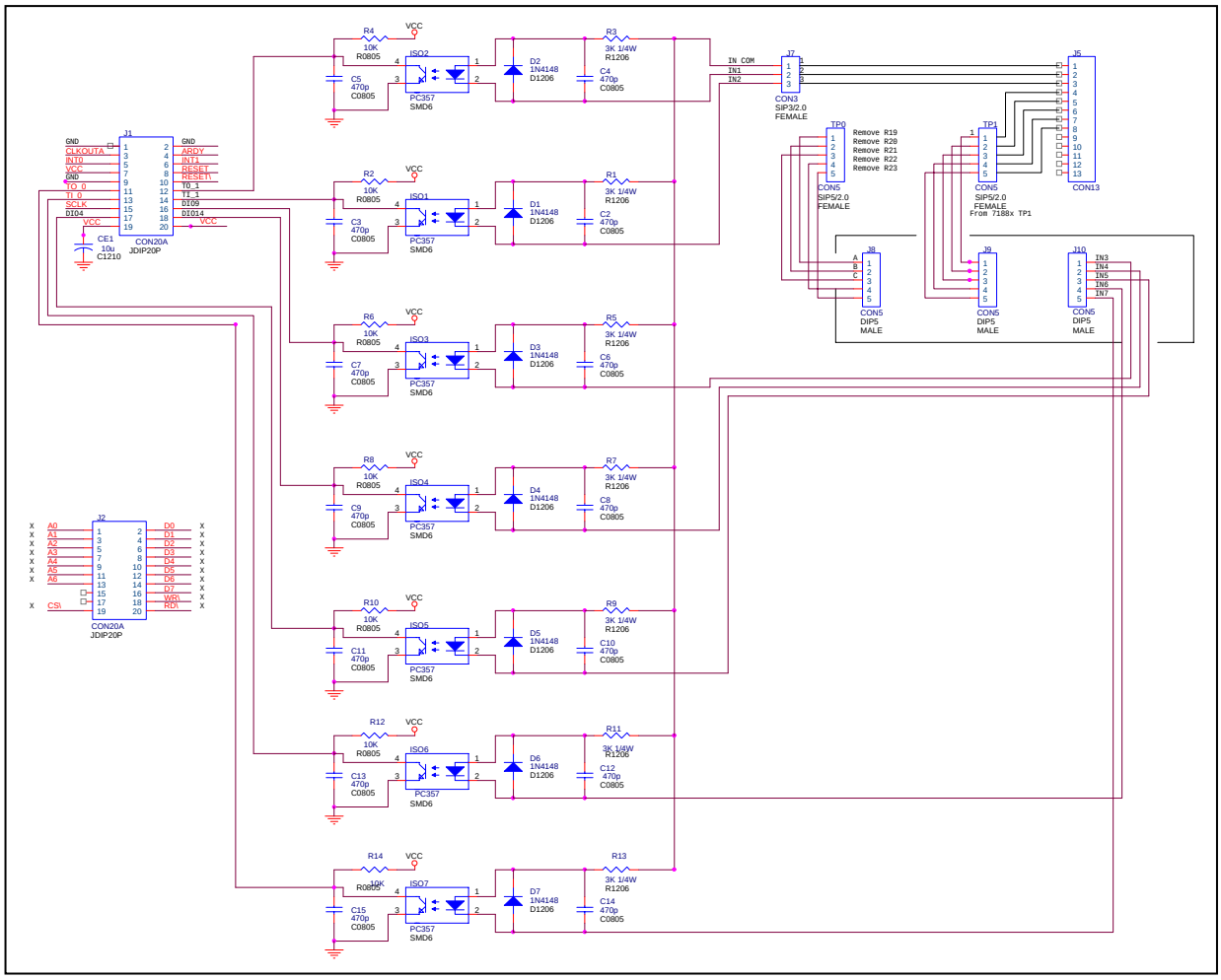
3.5.3 Block Diagram



3.5.4 Programming

```
SetTo10Dir(1);    XDI1=GetTo1();      // set to D/I & read D/I, channel_1
SetTi1Dir(1);         XDI2=GetTi1();      // set to D/I & read D/I, channel_2
SetDio9Dir(1);    XDI3=GetDio9();     // set to D/I & read D/I, channel_3
SetDio14Dir(1);   XDI4=GetDio14();        // set to D/I & read D/I, channel_4
SetDio4Dir(1);    XDI5=GetDio4();     // set to D/I & read D/I, channel_5
SetTi0Dir(1);         XDI6=GetTi0();      // set to D/I & read D/I, channel_6
SetTo0Dir(1);     XDI7=GetTo0();      // set to D/I & read D/I, channel_7
```

3.5.5 Circuit Diagram

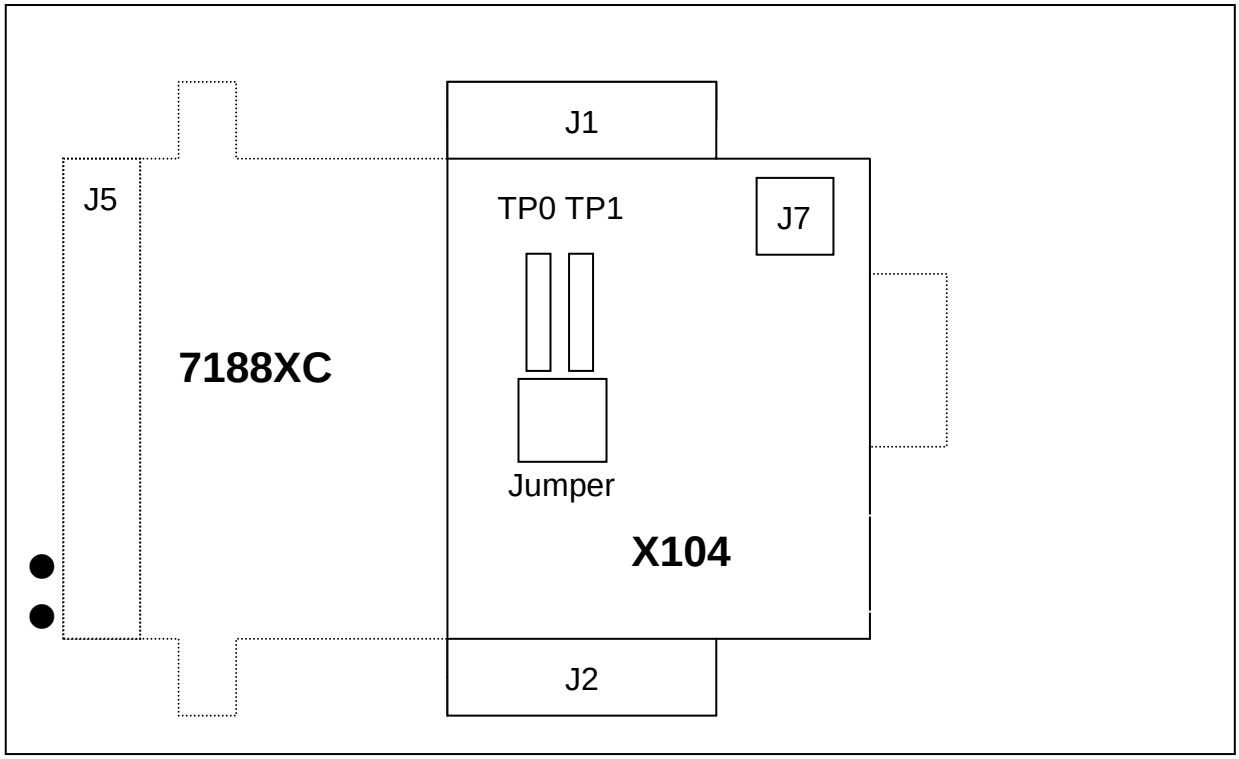


3.6 X104: D/I/O * 8, single-bit

3.6.1 Specifications

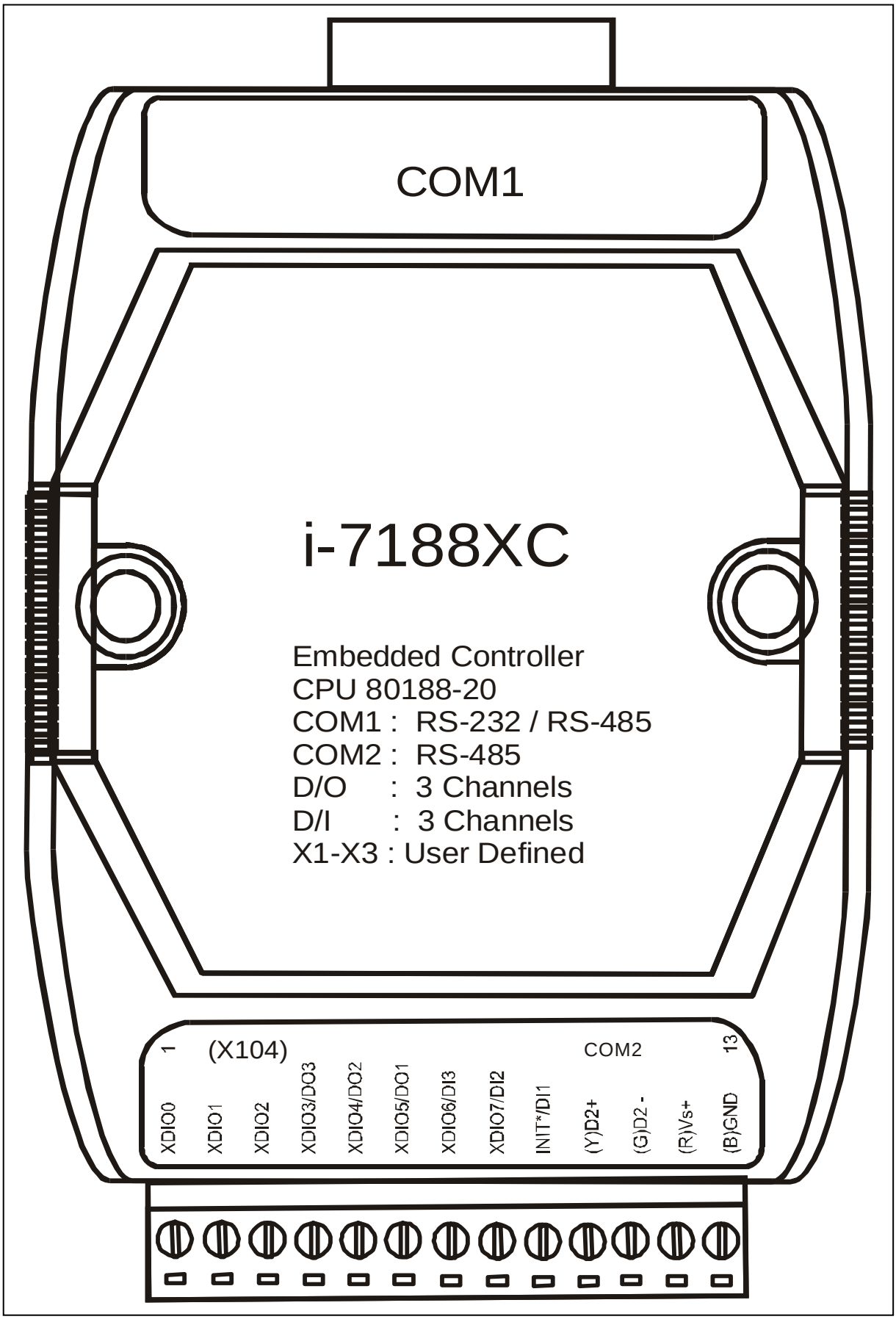
- 8 channels of D/I/O (single channel programmable)
- For 7188XC series

3.6.2 Pin Assignment & Jumper Setting

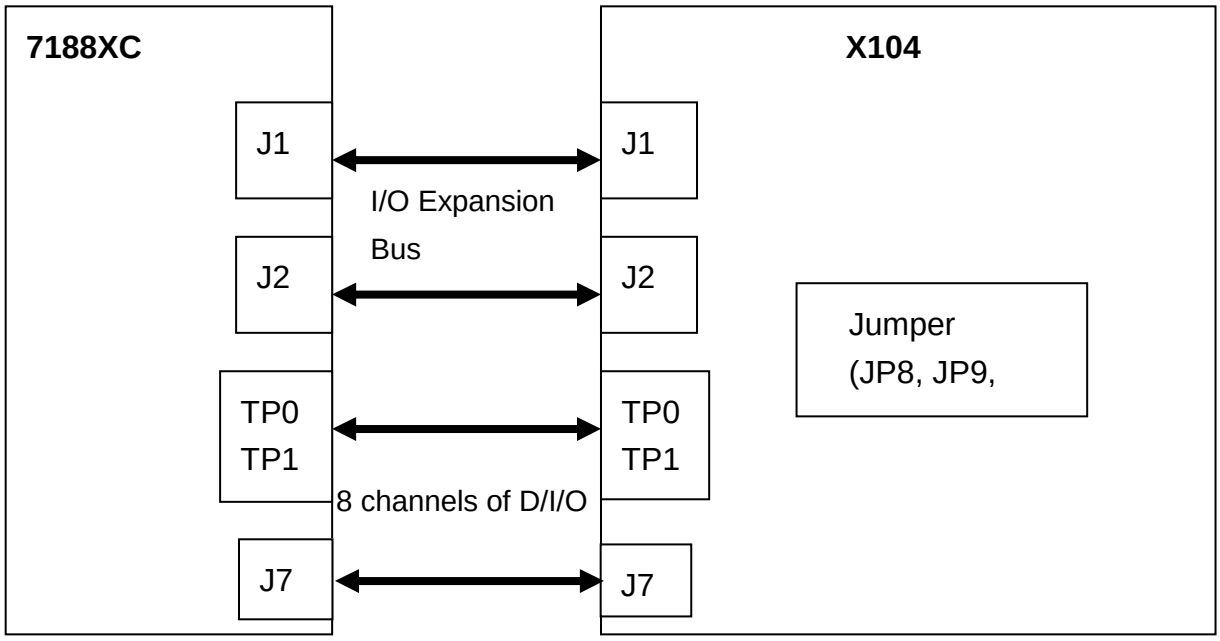


- **Note: user should remove R19, R20, R21, R22 and R23 in the 7188XC first.**
- **J1:** I/O expansion bus, connect to J1 of 7188XC
- **J2:** I/O expansion bus, connect to J2 of 7188XC
- **J7:** Three channels of 8 D/I/O
- **TP0:** Original function on 7188XC
- **TP1:** Five channels of 8 D/I/O
- **Jumper:** Select **TP0** or **TP1** function
  - **TP0:** JP9 and JP8 closeed
  - **TP1:** JP9 and JP10 closed
- **J5:** The pin assignment of J5 is given as follows: (the pin assignment will be different based on different jumper setting)

XDI4 initial state must be High. If its initial state is LOW, system clock will be reduced to 10M. So all clock-related libraries will be only half-speed.


COM1
i-7188XC
Embedded Controller
CPU 80188-20
COM1 : RS-232 / RS-485
COM2 : RS-485
D/O : 3 Channels
D/I : 3 Channels
X1-X3 : User Defined
1
(X104)
COM2
13
XDIO0
XDIO1
XDIO2
XDIO3/DO3
XDIO4/DO2
XDIO5/DO1
XDIO6/DI3
XDIO7/DI2
INIT*/DI1
(Y)D2+
(G)D2 -
(R)Vs+
(B)GND

3.6.3 Block Diagram



3.6.4 Programming

- Refer to C:\7188xc\demo\ioexpbus\X104*.* for demo program

- Software library

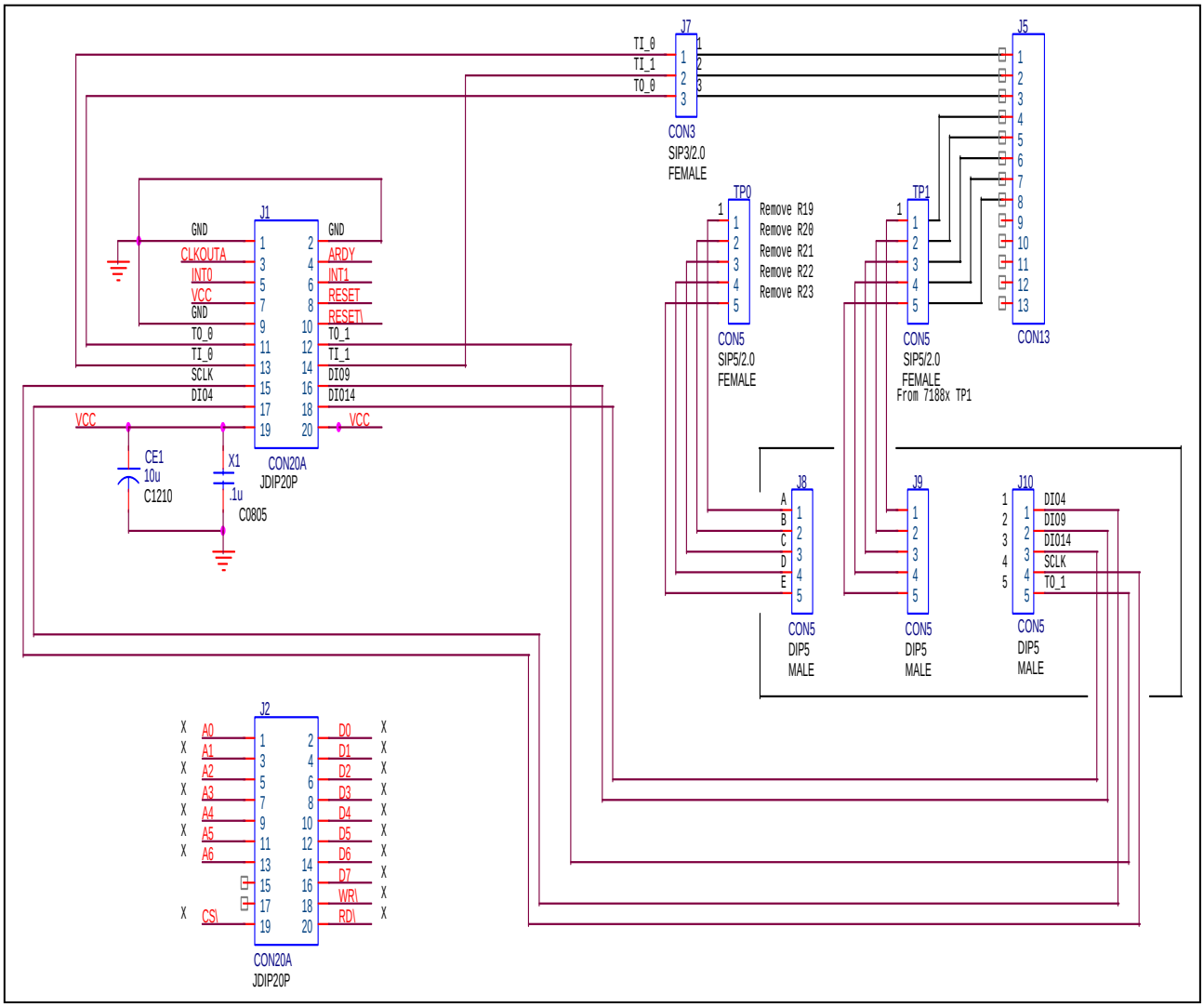
void SetDio4Dir(int dir);
void SetDio4High(void);
void SetDio4Low(void);
int GetDio4(void);

void SetDio9Dir(int dir);
void SetDio9High(void);
void SetDio9Low(void);
int GetDio9(void);

void SetDio14Dir(int dir);
void SetDio14High(void);
void SetDio14Low(void);
int GetDio14(void);

```
void SetTi1Dir(int dir);
void SetTi1High(void);
void SetTi1Low(void);
int GetTi1(void);

void SetTo1Dir(int dir);
void SetTo1High(void);
void SetTo1Low(void);
int GetTo1(void);

void SetTi0Dir(int dir);
void SetTi0High(void);
void SetTi0Low(void);
int GetTi0(void);

void SetTo0Dir(int dir);
void SetTo0High(void);
void SetTo0Low(void);
int GetTo0(void);

void SetDo1High(void);
void SetDo1Low(void);
int GetDo1(void);

void SetDo2High(void);
void SetDo2Low(void);
int GetDo2(void);

void SetDo3High(void);
void SetDo3Low(void);
int GetDo3(void);

int GetDi2(void);
int GetDi3(void);

void ClockHighLow(void);
void ClockHigh(void);
void ClockLow(void);
```

3.6.5 Circuit Diagram

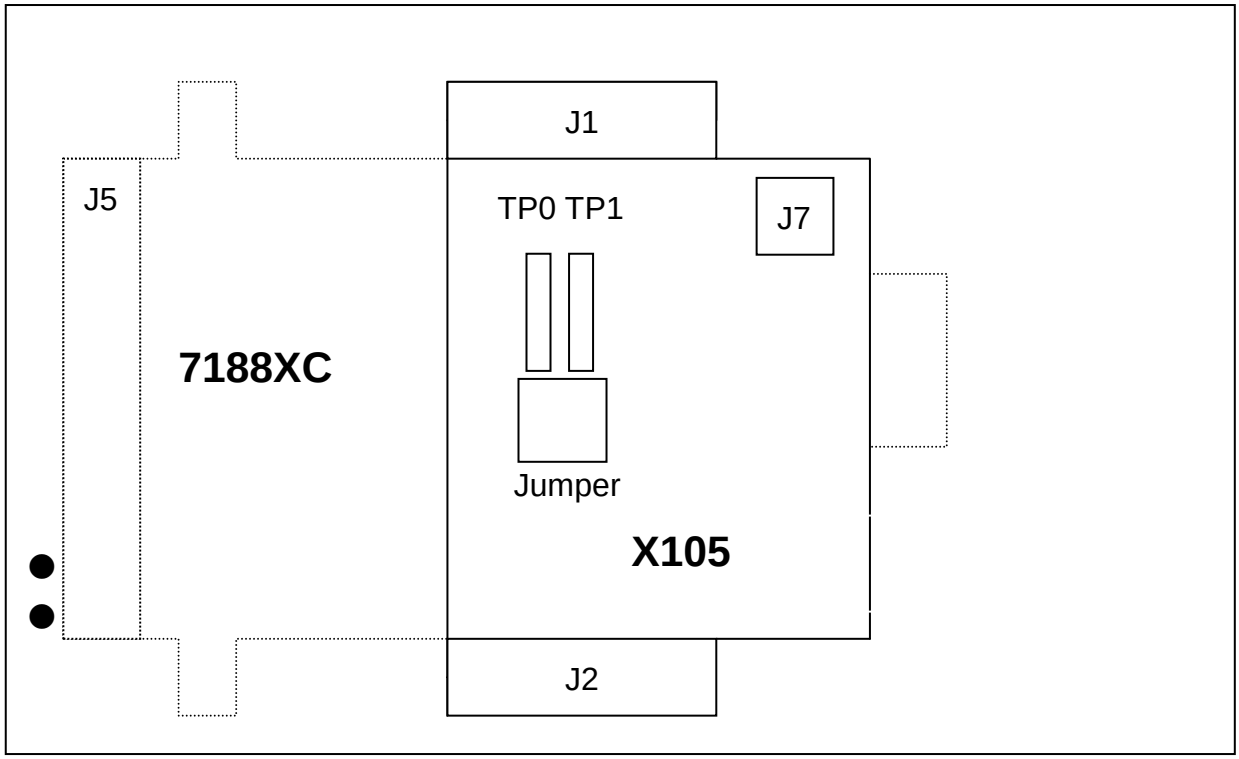


3.7 X105 D/I/O * 8, 8-bit

3.7.1 Specifications

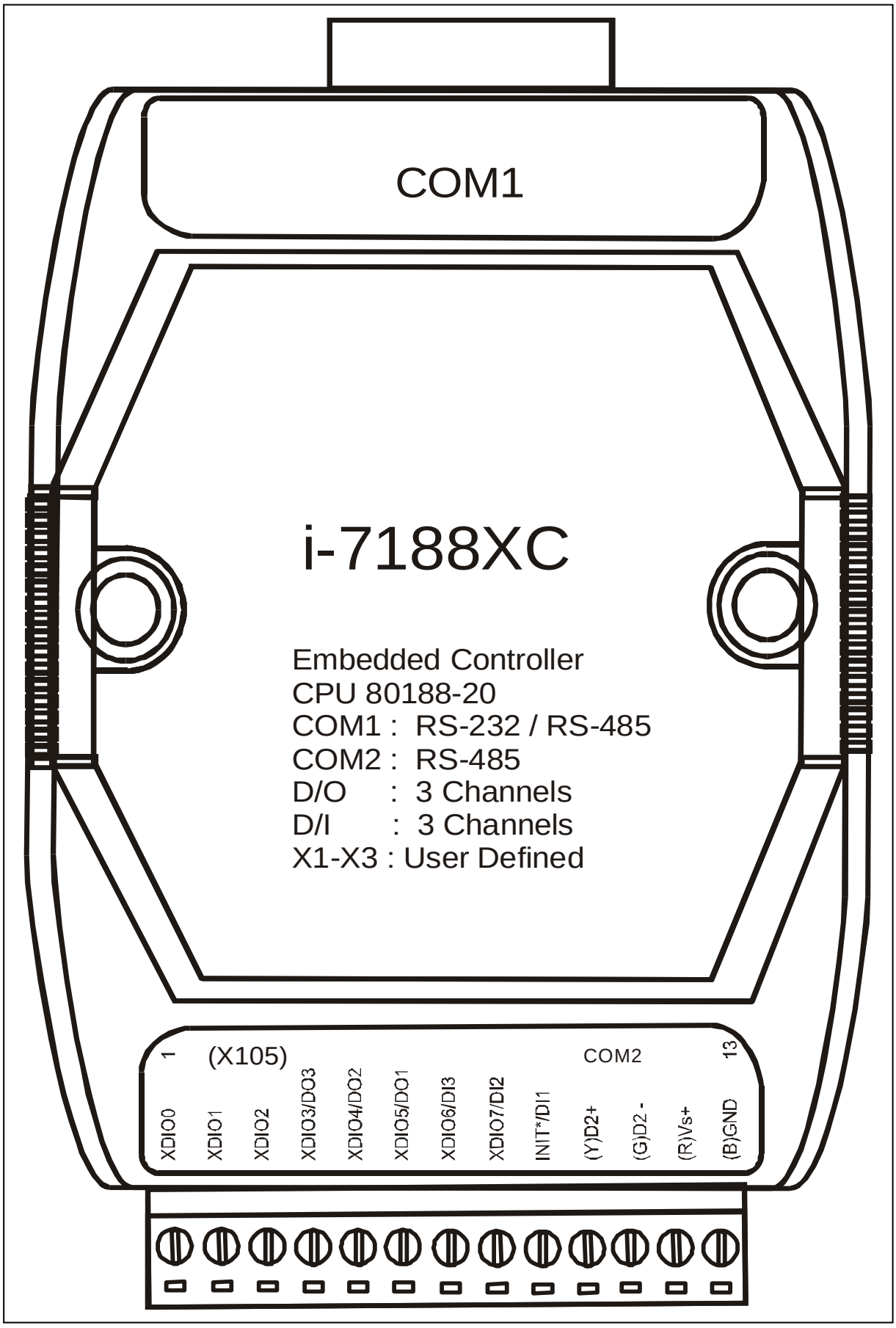
- 8 channels of D/I/O (8-channels programmable)
- For 7188XC series

3.7.2 Pin Assignment & Jumper Setting

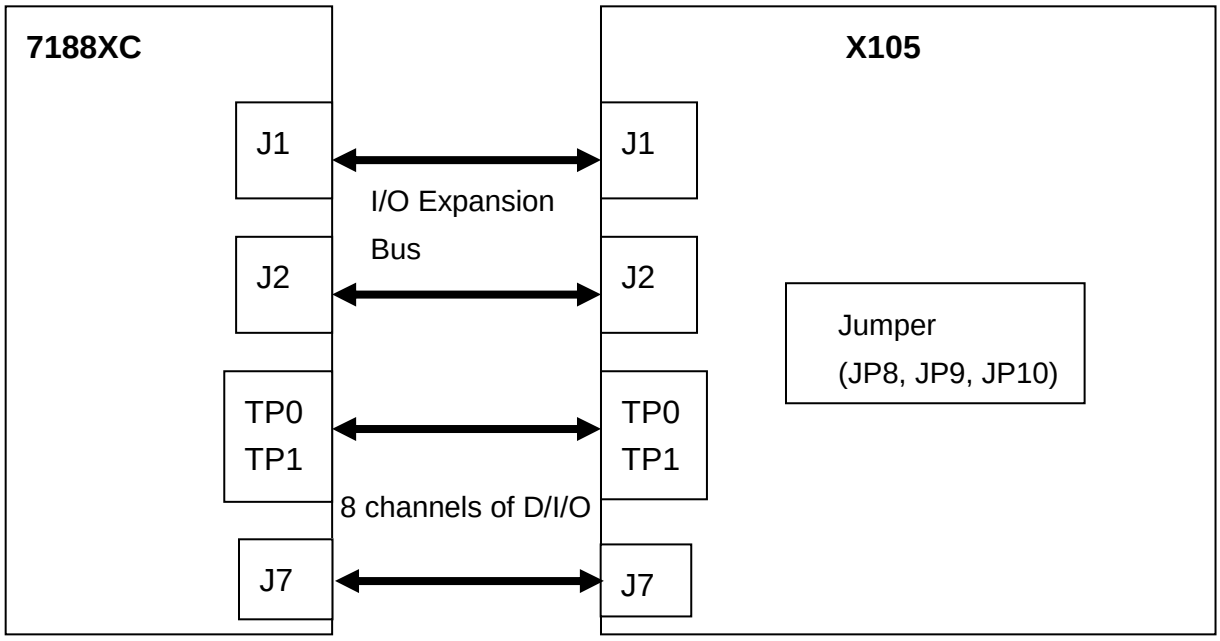


- **Note: user should remove R19, R20, R21, R22 and R23 in the 7188XC first.**
- **J1:** I/O expansion bus, connect to J1 of 7188XC
- **J2:** I/O expansion bus, connect to J2 of 7188XC
- **J7:** Three channels of 8 D/I/O
- **TP0:** Original function on 7188XC
- **TP1:** Five channels of 8 D/I/O
- **Jumper:** Select **TP0** or **TP1** function
  - **TP0:** JP9 and JP8 closed
  - **TP1:** JP9 and JP10 closed
- **J5:** The pin assignment of J5 is given as follows: (the pin assignment will be different based on different jumper setting)

XDI4 initial state must be High. If its initial state is LOW, system clock will be reduced to 10M. So all clock-related libraries will be only half-speed.


COM1
i-7188XC
Embedded Controller
CPU 80188-20
COM1 : RS-232 / RS-485
COM2 : RS-485
D/O : 3 Channels
D/I : 3 Channels
X1-X3 : User Defined
1
(X105)
COM2
13
XDIO0
XDIO1
XDIO2
XDIO3/DO3
XDIO4/DO2
XDIO5/DO1
XDIO6/DI3
XDIO7/DI2
INIT*/DI1
(Y)D2+
(G)D2 -
(R)Vs+
(B)GND

3.7.3 Block Diagram



3.7.4 Programming

DiVal = **inportb(BASE); /* for all 8-channels */**

Note: 1. The default value of BASE is 0.

2. It is **not** recommended to change the value of BASE from 0 to another value.

3. DiVal=0 → all 8-channel are Low
   DiVal=1 → Chennel_0 is High, the other channels are Low
   DiVal=0xff → all 8-channel are High

outportb(BASE, DoVal); /* for all 8-channels */

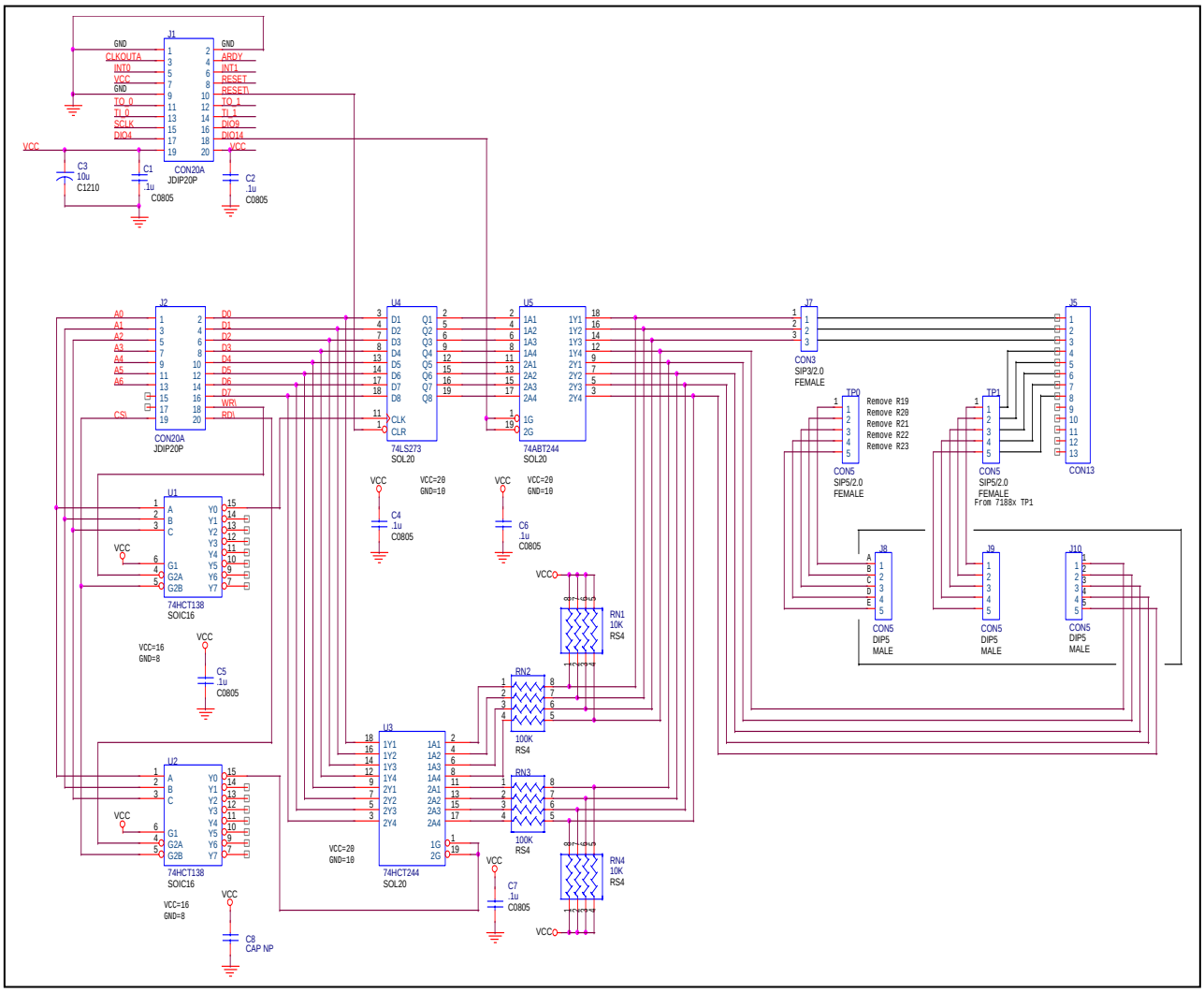
Note: 1. The default value of BASE is 0.

2. It is **not** recommended to change the value of BASE from 0 to another value.

3. DoVal=0 → turn all 8-channel OFF
   DoVal=1 → turn chennel_0 ON, the other channels OFF
   DoVal=0xff→ turn all 8-channel ON

Refer to next page for more information.

3.7.5 Circuit Diagram



- DIO14 is used to select D/I or D/O
- If DIO14 is **LOW → select D/O*8** → D/I is read-back value of D/O
- If DIO14 is **HIGH → select D/I*8** → D/I signals are come from J5

Select D/I*8 as following:

```
SetDio14Dir(0);          /* select DIO14 as D/O          */
SetDio14High();          /* select D/I*8                 */
DiVal=inportb(BASE);     /* read D/I*8 (from J5)     */
```

Select D/I*8 as following:

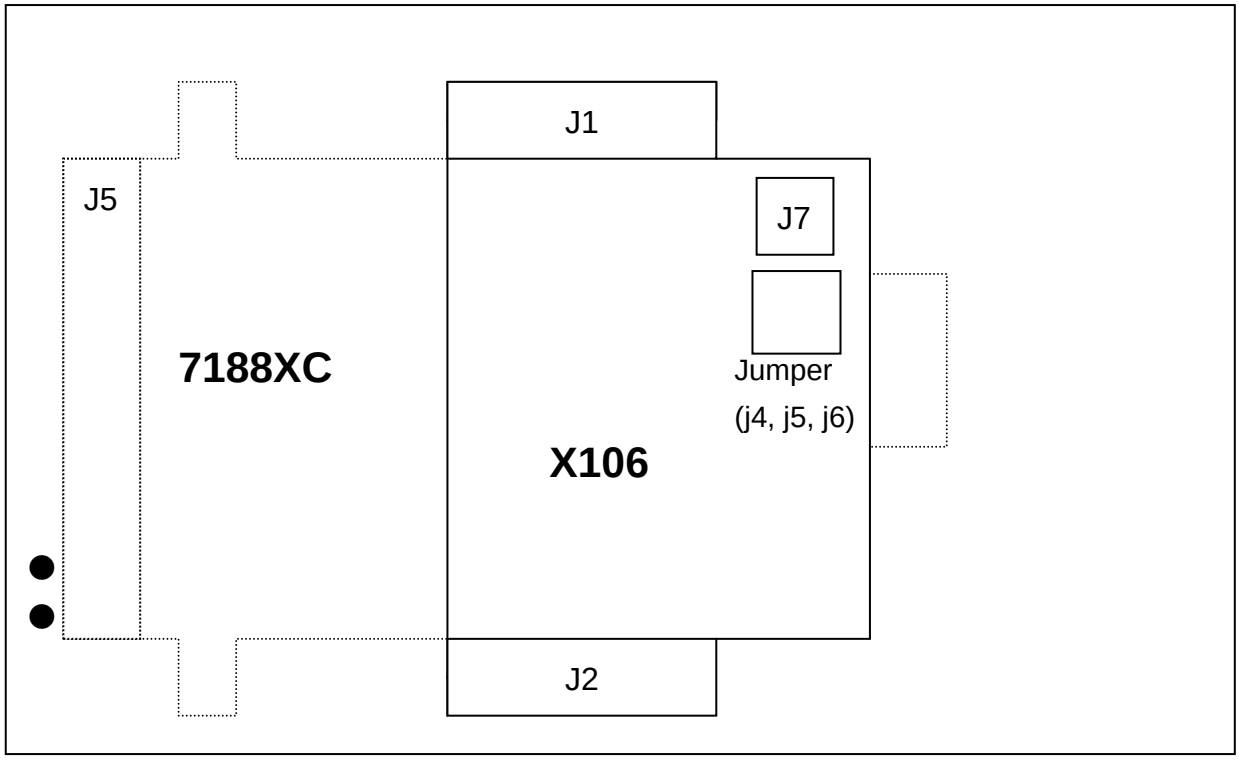
```
SetDio14Dir(0);          /* select DIO14 as D/O          */
SetDio14Low();           /* select D/O*8             */
outportb(BASE,DoVal);        /* set value of D/O*8 (to J5)   */
DiVal=inportb(BASE);     /* D/O*8  read back         */
```

3.8 X106 DO *2 | DI *3

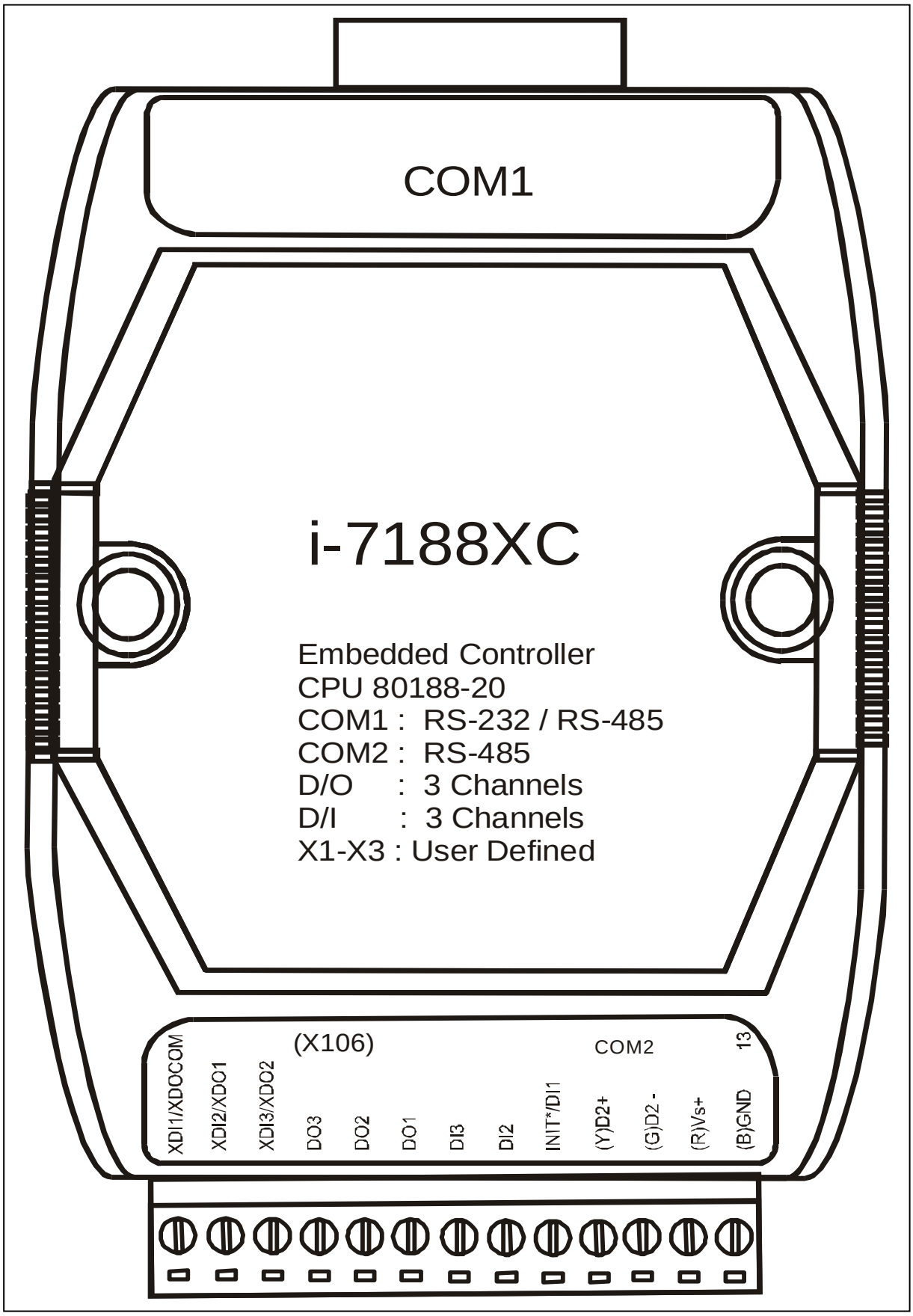
3.8.1 Specifications

- 2 channels of D/O (Open collector output, 30V, 250mA max.)
- Or 3 channels of DI, Logic high level: (3.5V~30V), Logic low level: (0V~1V)
- For 7188XC series

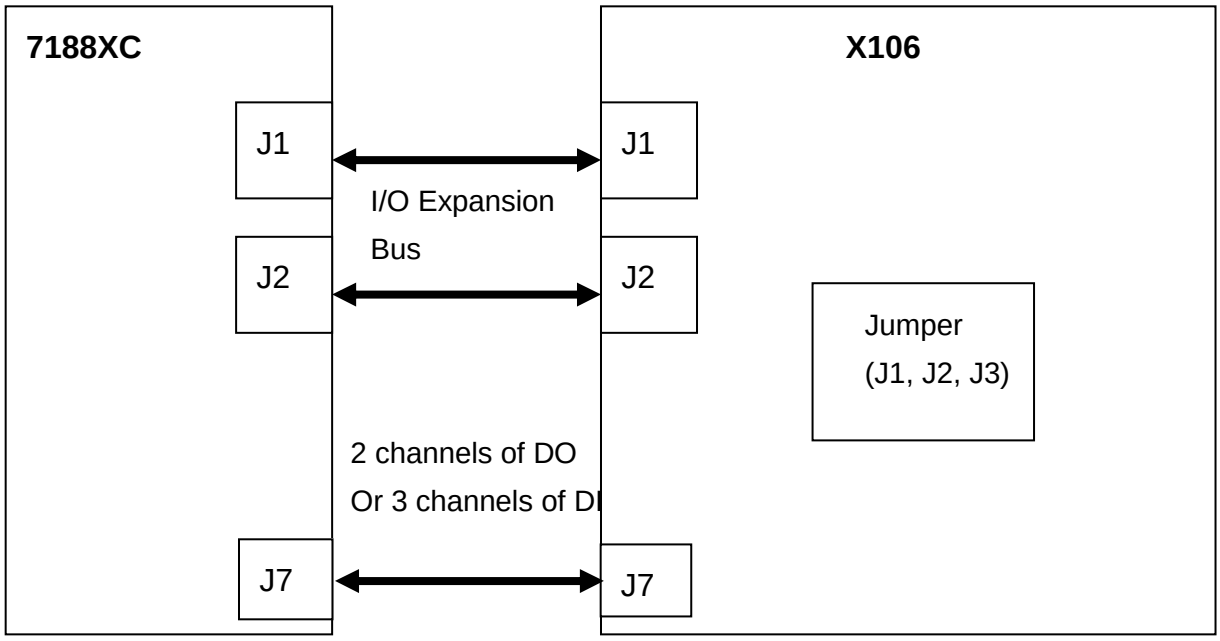
3.8.2 Pin Assignment & Jumper Setting



- **J1:** I/O expansion bus, connect to J1 of 7188XC
- **J2:** I/O expansion bus, connect to J2 of 7188XC
- **J7:** Three channels of D/I or two channels of D/O
- **Jumper:** Select **D/I** or **D/O** function
  D/I: j4, j5,j6 select 2-3 **(default setting)**
  D/O: j4, j5, j6 select 1-2
- **J5:** The pin assignment of J5 is given as follows: (the pin assignment will be different based on different jumper setting)


COM1
i-7188XC
Embedded Controller
CPU 80188-20
COM1 : RS-232 / RS-485
COM2 : RS-485
D/O : 3 Channels
D/I : 3 Channels
X1-X3 : User Defined
(X106)
COM2
13
XDI1/XDOCOM
XDI2/XDO1
XDI3/XDO2
DO3
DO2
DO1
DI3
DI2
INIT*/DI1
(Y)D2+
(G)D2 -
(R)Vs+
(B)GND

3.8.3 Block Diagram



3.8.4 Programming

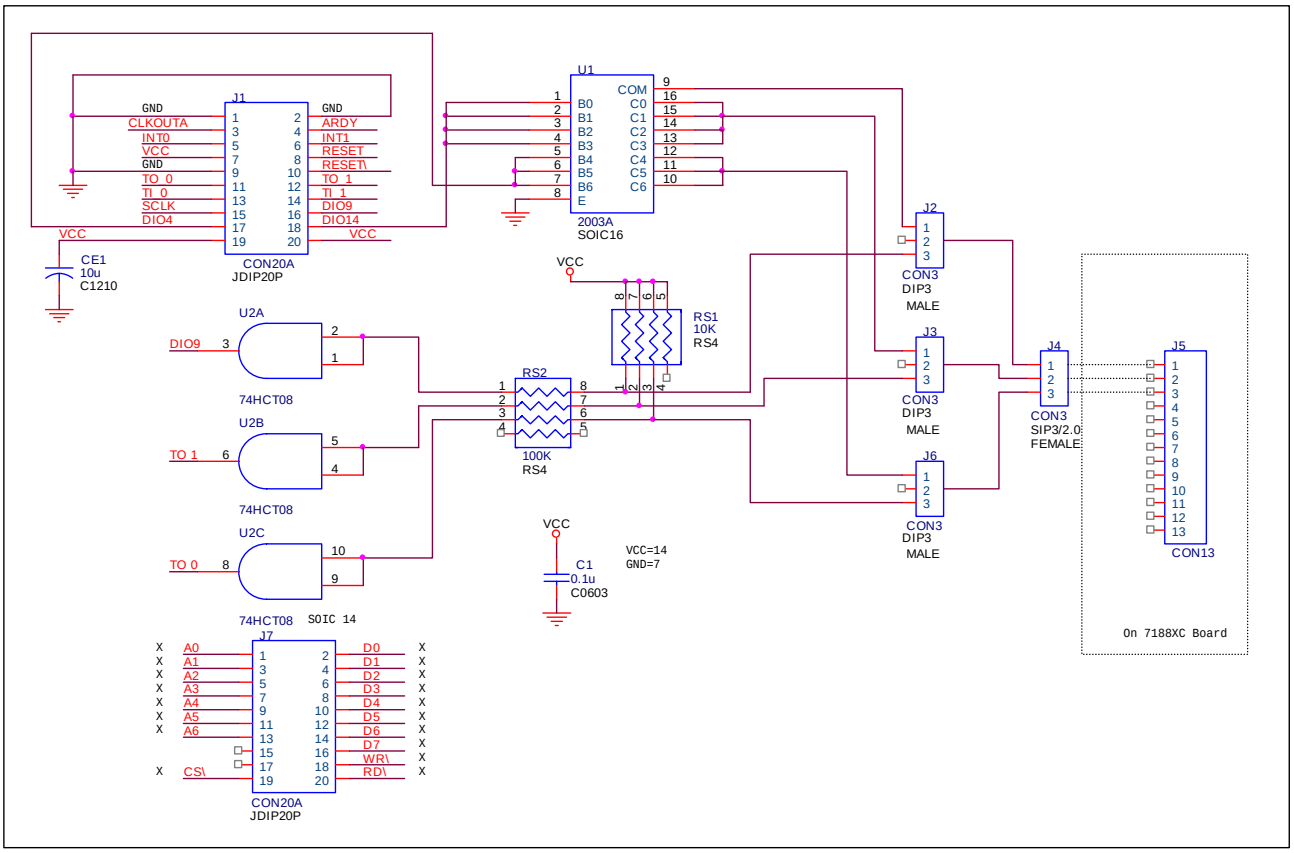
- ***DO***

```
SetDio4Dir( 0 );          // Set D/O channel_1
SetDio14Dir( 0 );         // Set D/O channel_2
SetDio4Low();             // Turn D/O channel_1 OFF
SetDio14Low();            // Turn D/O channel_2 OFF
 SetDio4High();           // Turn D/O channel_1 ON
SetDio14High();           // Turn D/O channel_2 ON
```

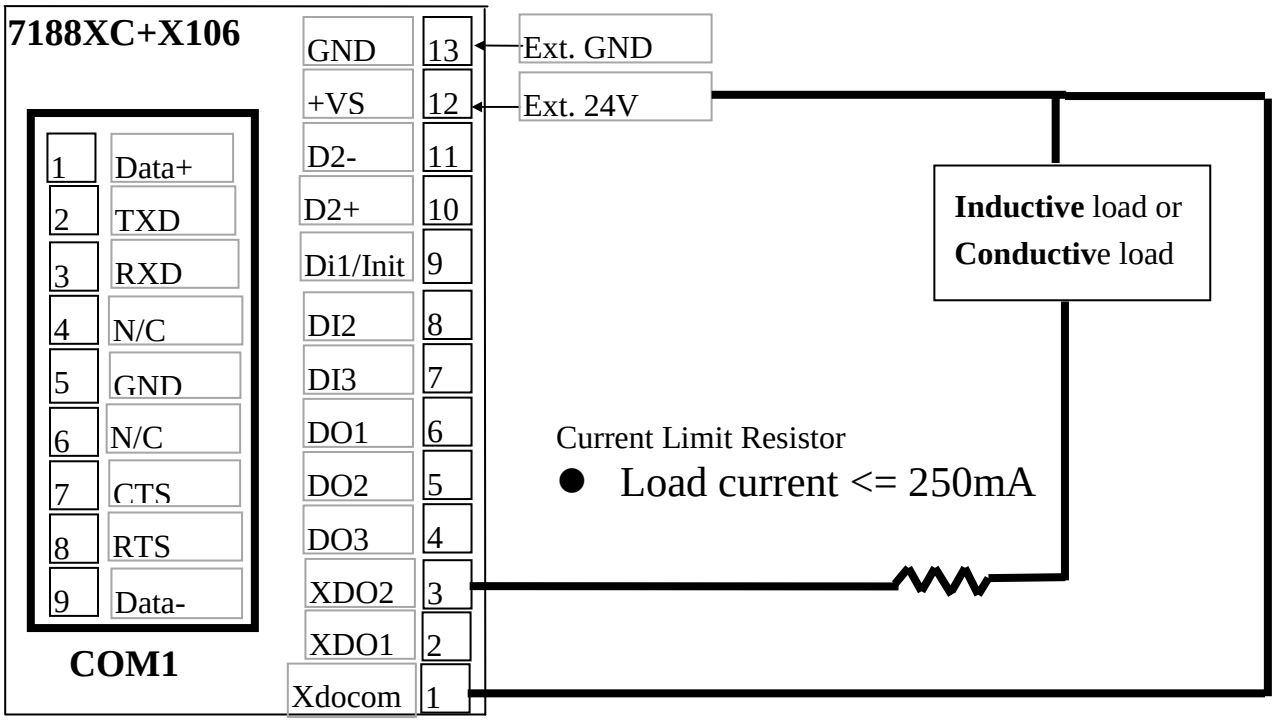
- ***DI***

```
Data = SetTo1Dir( 1 );    // Set D/I channel_1
Data = SetTo0Dir( 1 );    // Set D/I channel_2
Data = SetDio9Dir( 1 );   // Set D/I channel_3
Data = GetTo1Dir(  );     // Read D/I channel_1
Data = GetTo0Dir(  );     // Read D/I channel_2
Data = GetDio9Dir(  );    // Read D/I channel_3
```

3.8.5 Circuit Diagram



- If (j4,j5,j6) select D/O

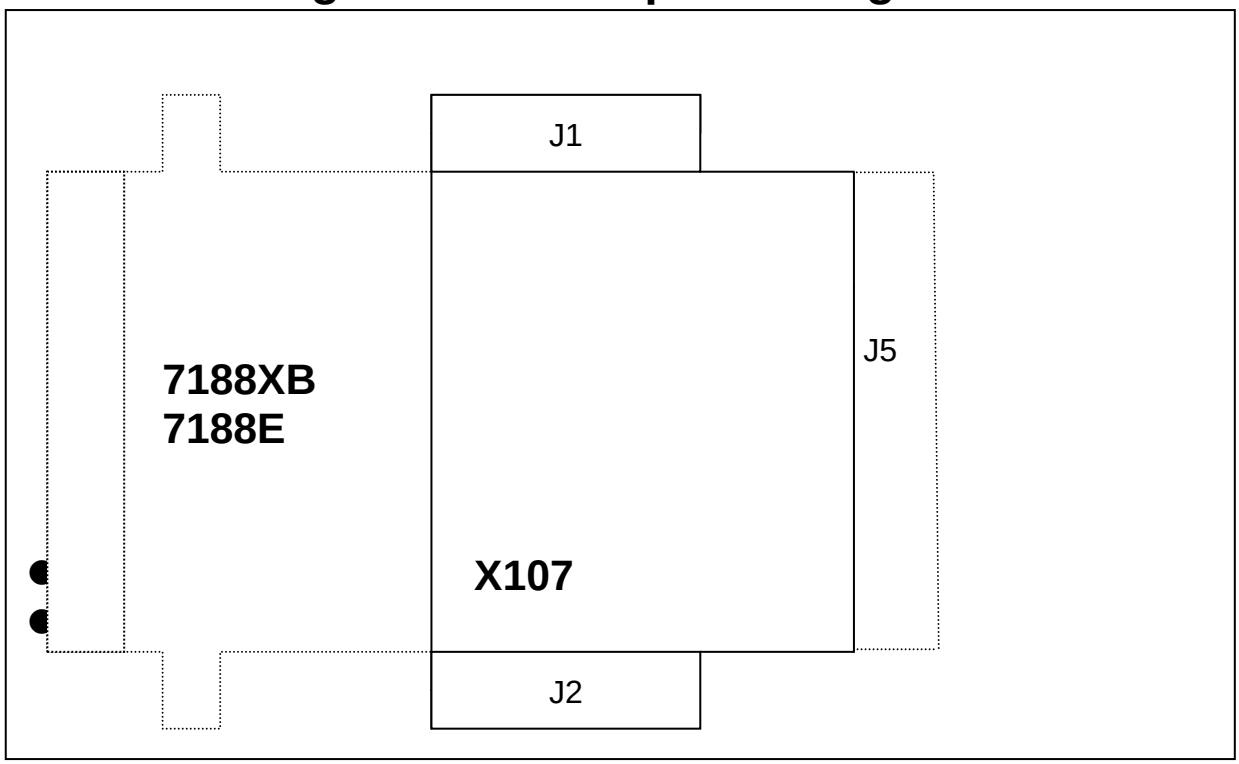


3.9 X107 DI *6 & DO *7

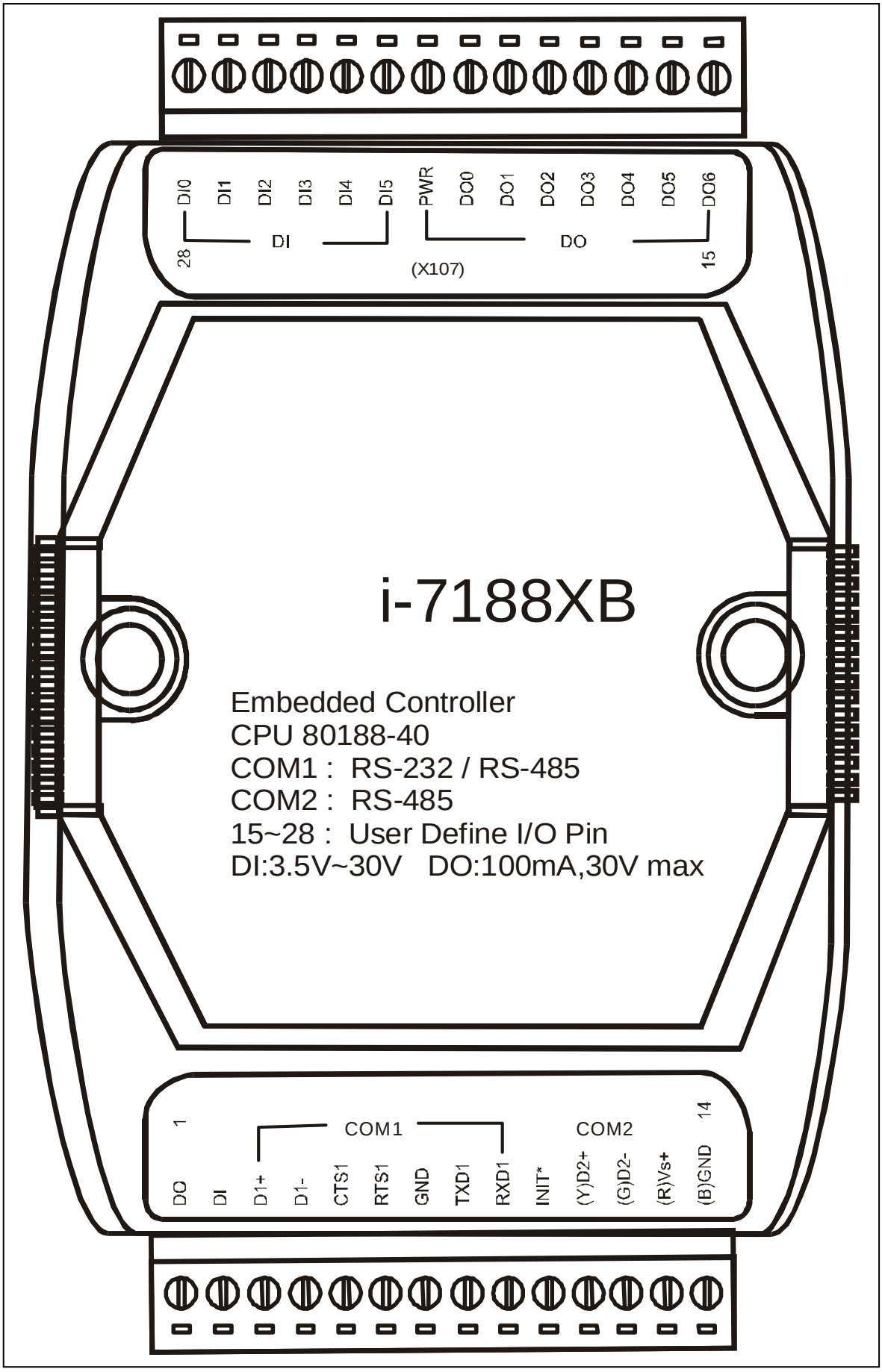
3.9.1 Specifications

- 7 channels of D/O, Open collector, 30V, 100mA max.
- 6 channels of D/I, Logic high level: (3.5V~30V), Logic low level: (0V~1V)
- For 7188XB/7188E

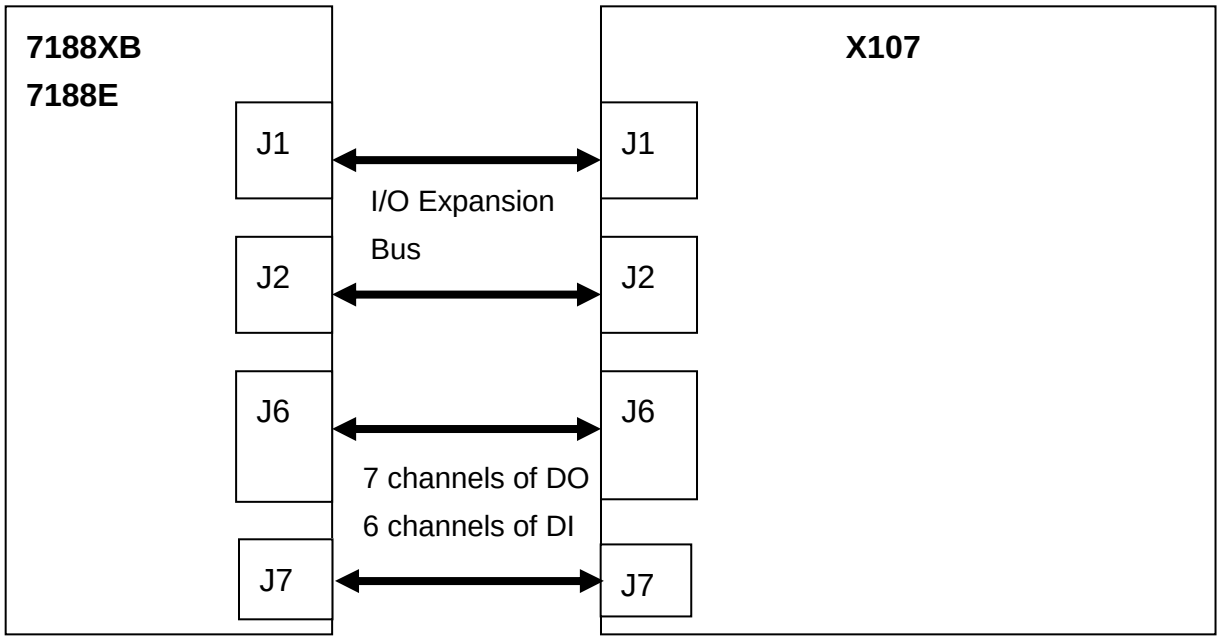
3.9.2 Pin Assignment & Jumper Setting



- **Note: refer to Sec. 1.5.6 of "7188XA/B/C & 7521/2/3 Hardware User's Manual" for I/O wire connection.**
- **J1:** I/O expansion bus, connect to J1 of 7188XB/7188E
- **J2:** I/O expansion bus, connect to J2 of 7188XB/7188E
- **J5:** The pin assignment is given as follows:


DI0
DI1
DI2
DI3
DI4
DI5
PWR
DO0
DO1
DO2
DO3
DO4
DO5
DO6
28
DI
DO
15
(X107)
i-7188XB
Embedded Controller
CPU 80188-40
COM1 : RS-232 / RS-485
COM2 : RS-485
15~28 : User Define I/O Pin
DI:3.5V~30V DO:100mA,30V max
1
COM1
COM2
14
DO
DI
D1+
D1-
CTS1
RTS1
GND
TXD1
RXD1
INIT*
(Y)D2+
(G)D2-
(R)Vs+
(B)GND

3.9.3 Block Diagram



3.9.4 Programming

DiVal = **inportb(BASE); /* for all 8-channels */**

Note: 1. The default value of BASE is 1.

2. It is **not** recommended to change the value of BASE from 0 to another value.

3. DiVal=0 → all 8-channel are Low
   DiVal=1 → Chennel_0 is High, the other channels are Low
   DiVal=0xff → all 8-channel are High

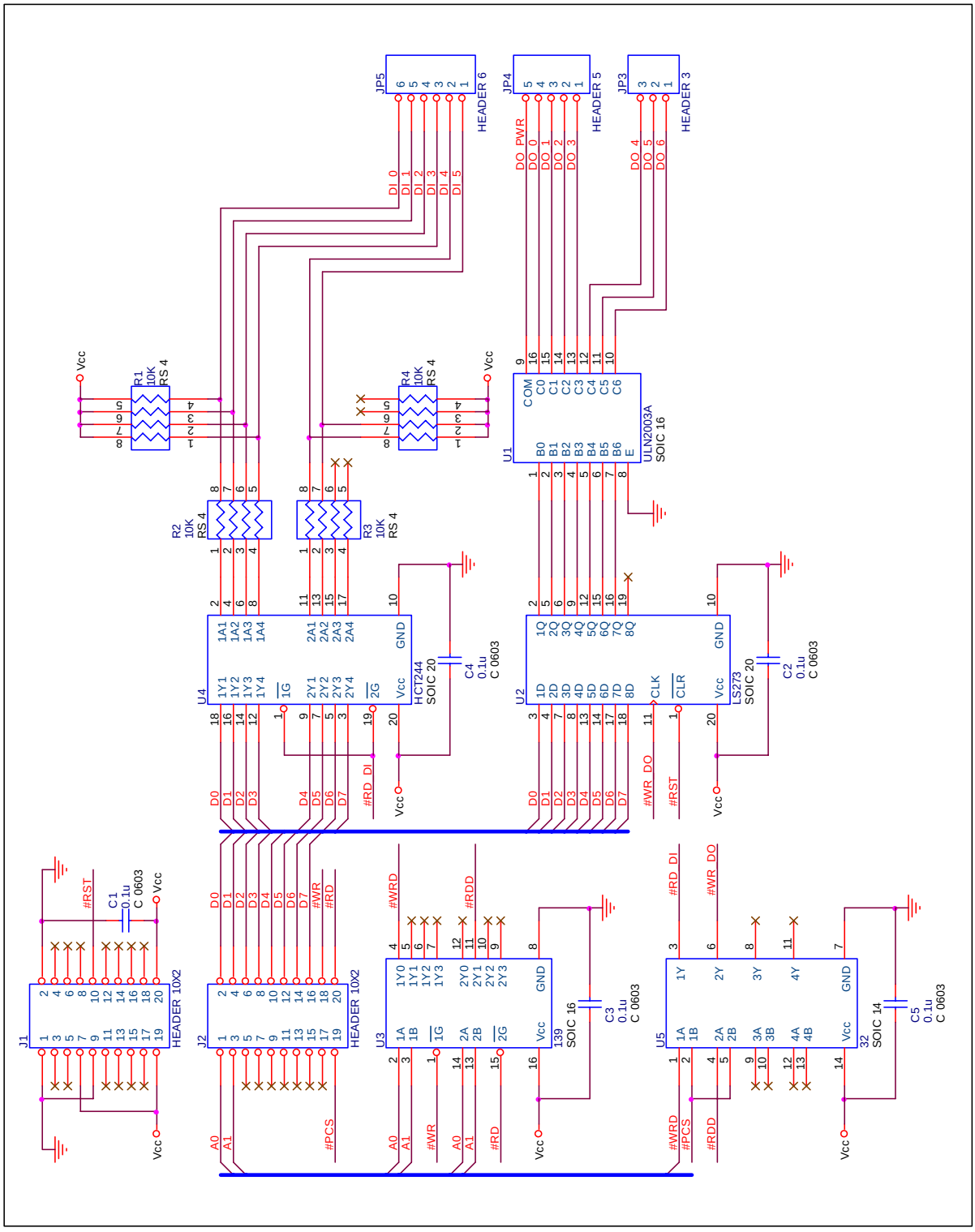
outportb(BASE, DoVal); /* for all 8-channels */

Note: 1. The default value of BASE is 0.

2. It is **not** recommended to change the value of BASE from 0 to another value.

3. DoVal=0 → turn all 8-channel OFF
   DoVal=1 → turn chennel_0 ON, the other channels OFF
   DoVal=0xff → turn all 8-channel ON

3.9.5 Circuit Diagram

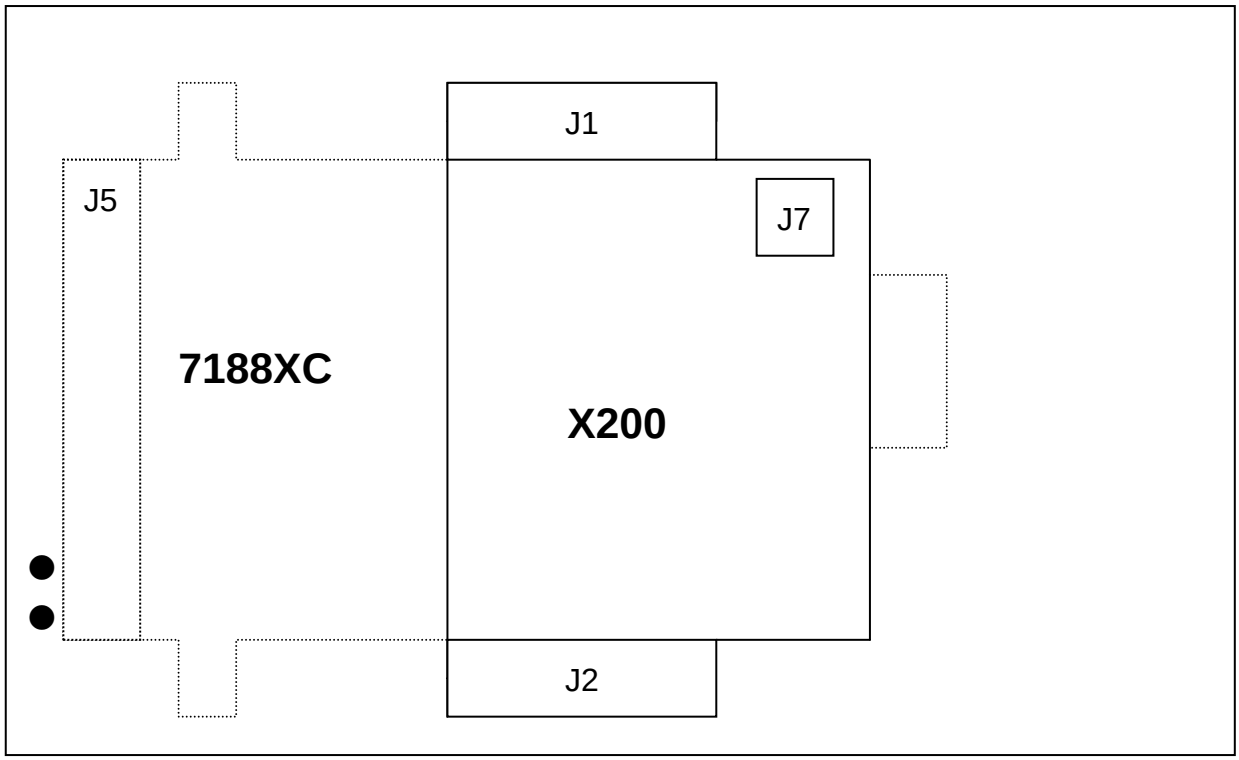


X200 A/D *1

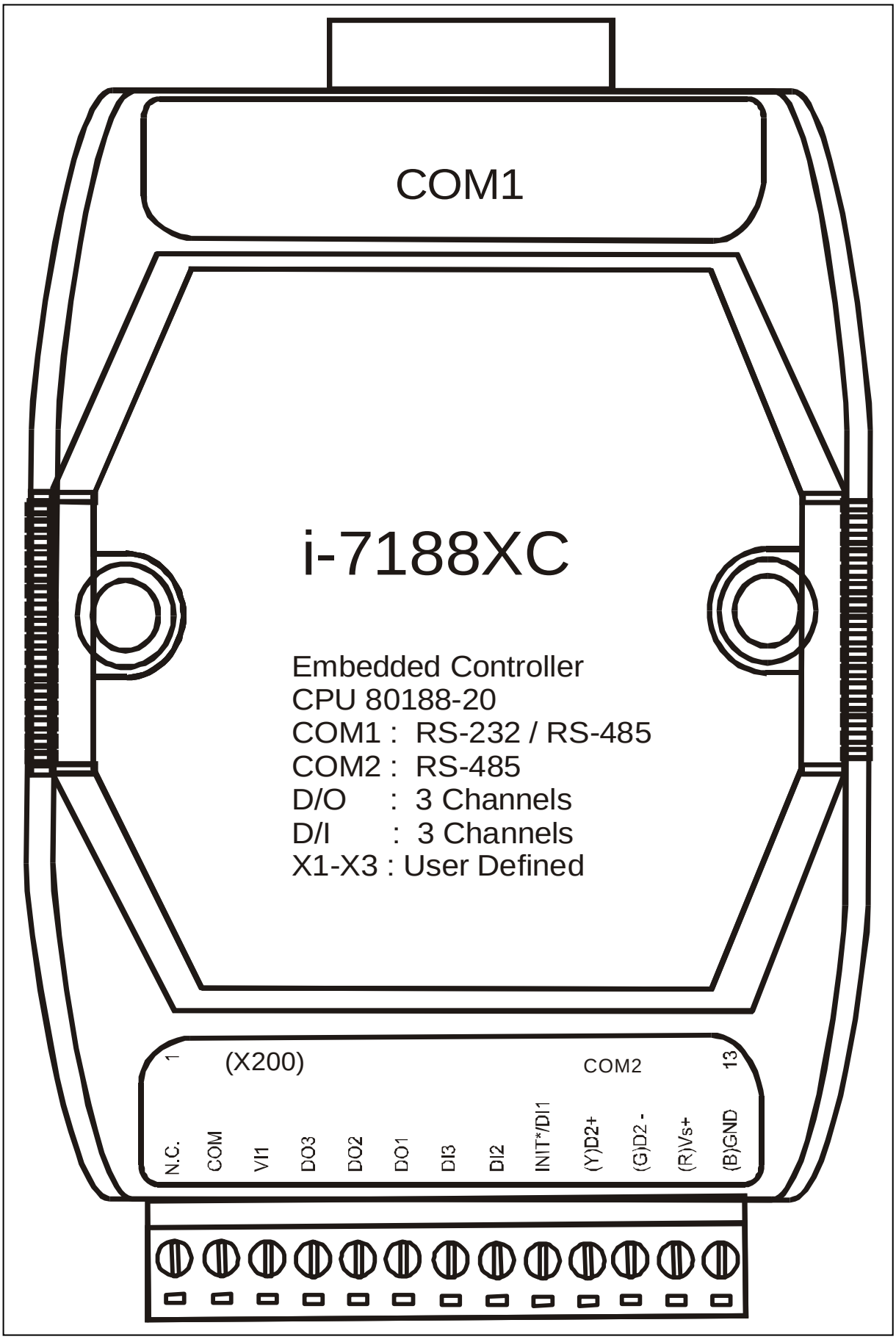
3.9.6 Specifications

- 1 channel of A/D (0-2.5v, 12 bit)
- For 7188XC series

3.9.7 Pin Assignment & Jumper Setting



- **J1:** I/O expansion bus, connect to J1 of 7188XC
- **J2:** I/O expansion bus, connect to J2 of 7188XC
- **J7:** One channel of A/D
- **J5:** The pin assignment is given as follows:


COM1
i-7188XC
Embedded Controller
CPU 80188-20
COM1 : RS-232 / RS-485
COM2 : RS-485
D/O : 3 Channels
D/I : 3 Channels
X1-X3 : User Defined
1
(X200)
COM2
13
N.C.
COM
VI1
DO3
DO2
DO1
DI3
DI2
INIT*/DI1
(Y)D2+
(G)D2-
(R)Vs+
(B)GND

3.9.8 Programming

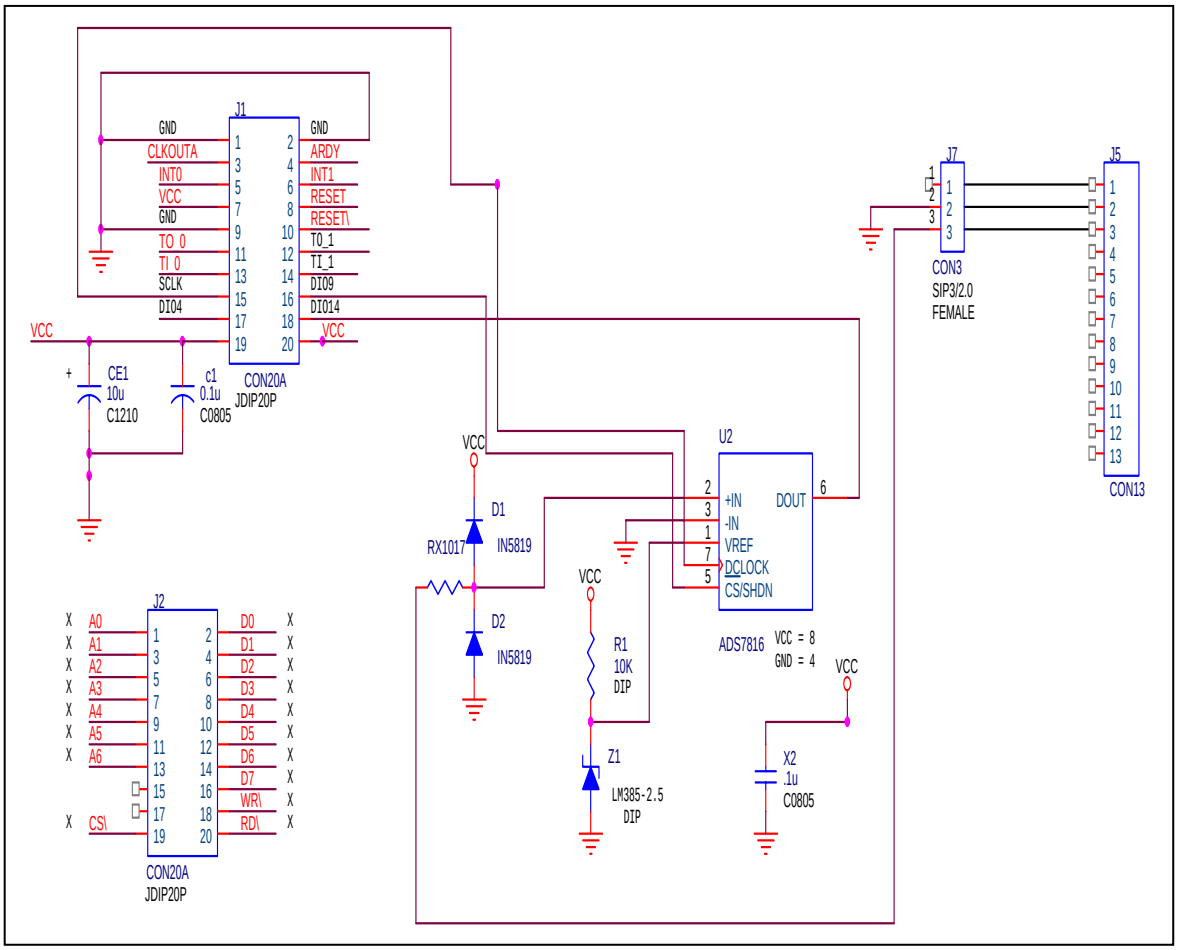
int AnalogIn(void)

Return value= 0 - 4095

Mapping formula: Vref / 4096 (Note: Vref=2.5v)

- Refer to C:\7188xc\demo\ioexpbus\X200*.* for demo program

3.9.9 Circuit Diagram

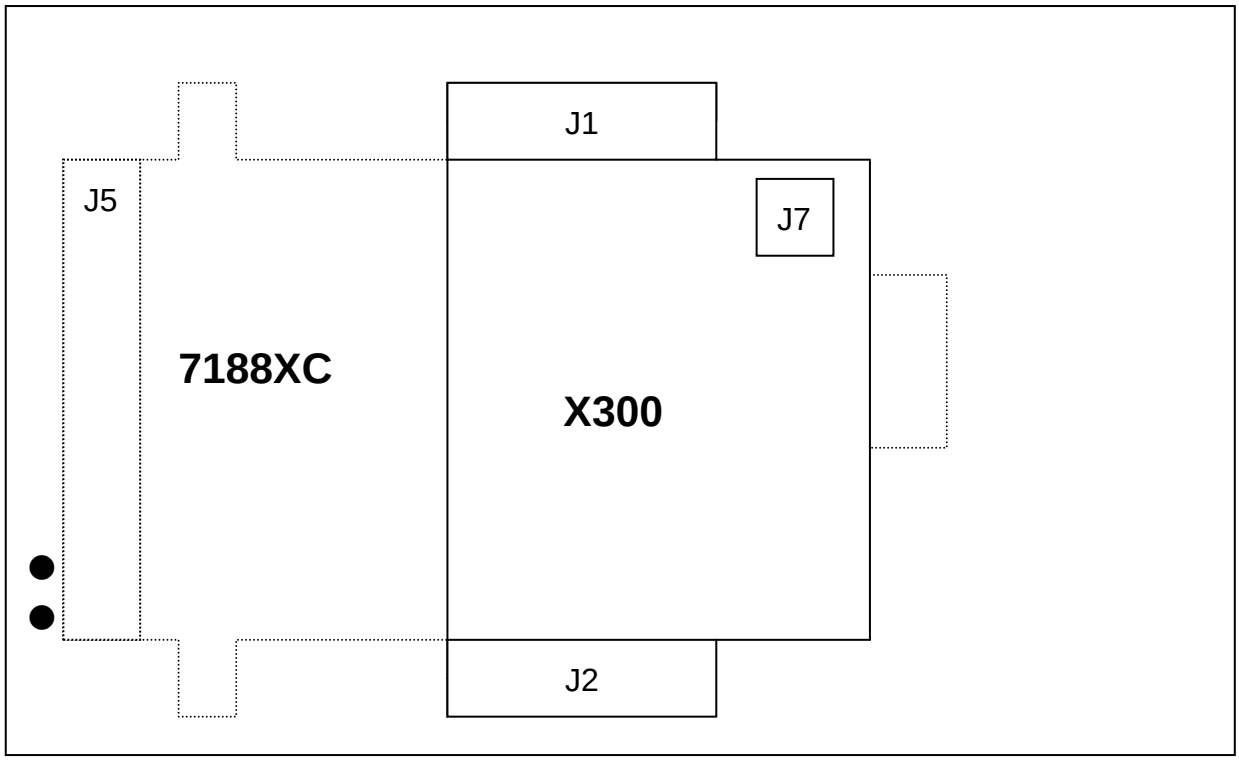


3.10 X300 D/A *2

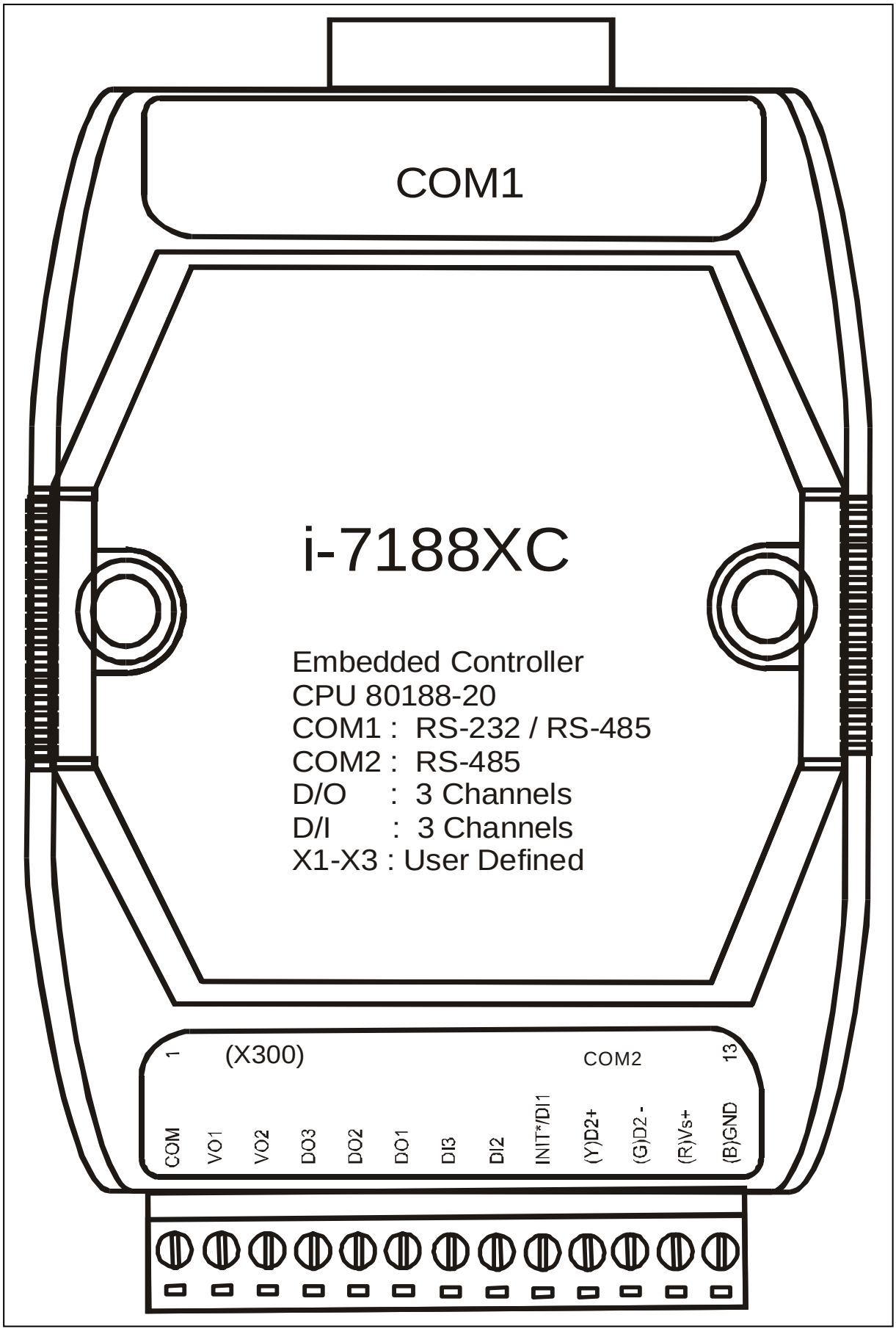
3.10.1 Specifications

- 2 channels of 12 bit D/A (0-4.095v)
- For 7188XC series

3.10.2 Pin Assignment & Jumper Setting



- **J1:** I/O expansion bus, connect to J1 of 7188XC
- **J2:** I/O expansion bus, connect to J2 of 7188XC
- **J7:** Two channels of 12 bit D/A
- **J5:** The pin assignment is given as follows:


COM1
i-7188XC
Embedded Controller
CPU 80188-20
COM1 : RS-232 / RS-485
COM2 : RS-485
D/O : 3 Channels
D/I : 3 Channels
X1-X3 : User Defined
1
(X300)
COM2
13
COM
VO1
VO2
DO3
DO2
DO1
DI3
DI2
INIT*/DI1
(Y)D2+
(G)D2 -
(R)Vs+
(B)GND

3.10.3 Programming

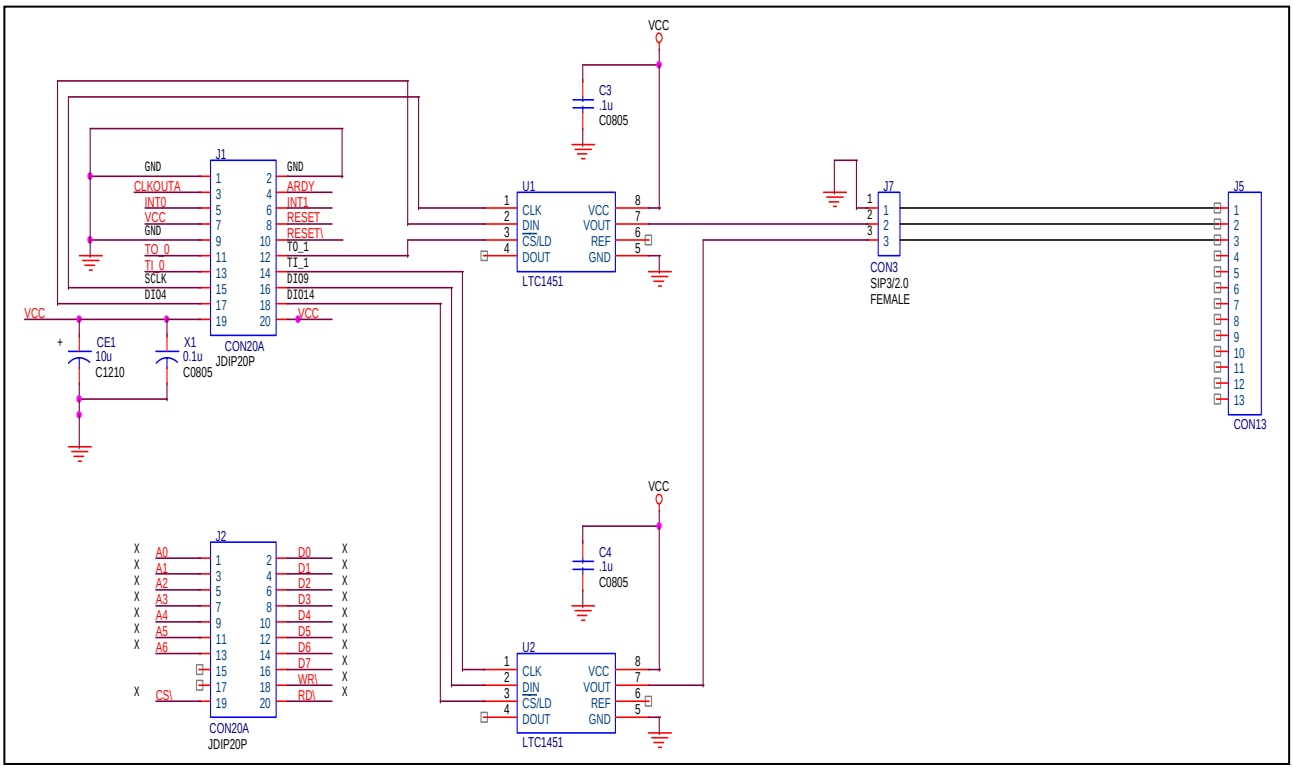
void AnalogOutput(int channel, int DataIn)

Channel = 0 or 1

DataIn = 0 – 4095 (note 4095→ 4.095V)

- Refer to C:\7188xc\demo\ioexpbus\X300*.* for demo program

3.10.4 Circuit Diagram

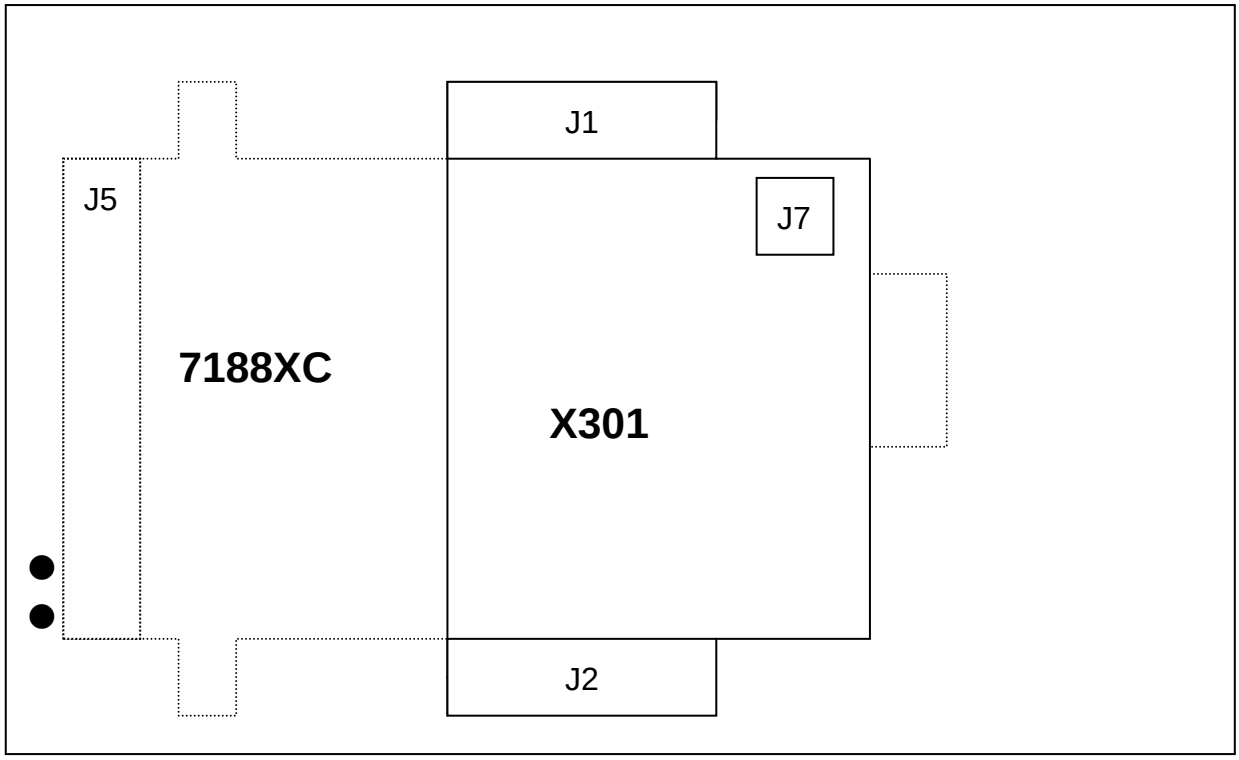


3.11 X301 D/A * 1 & A/D *1

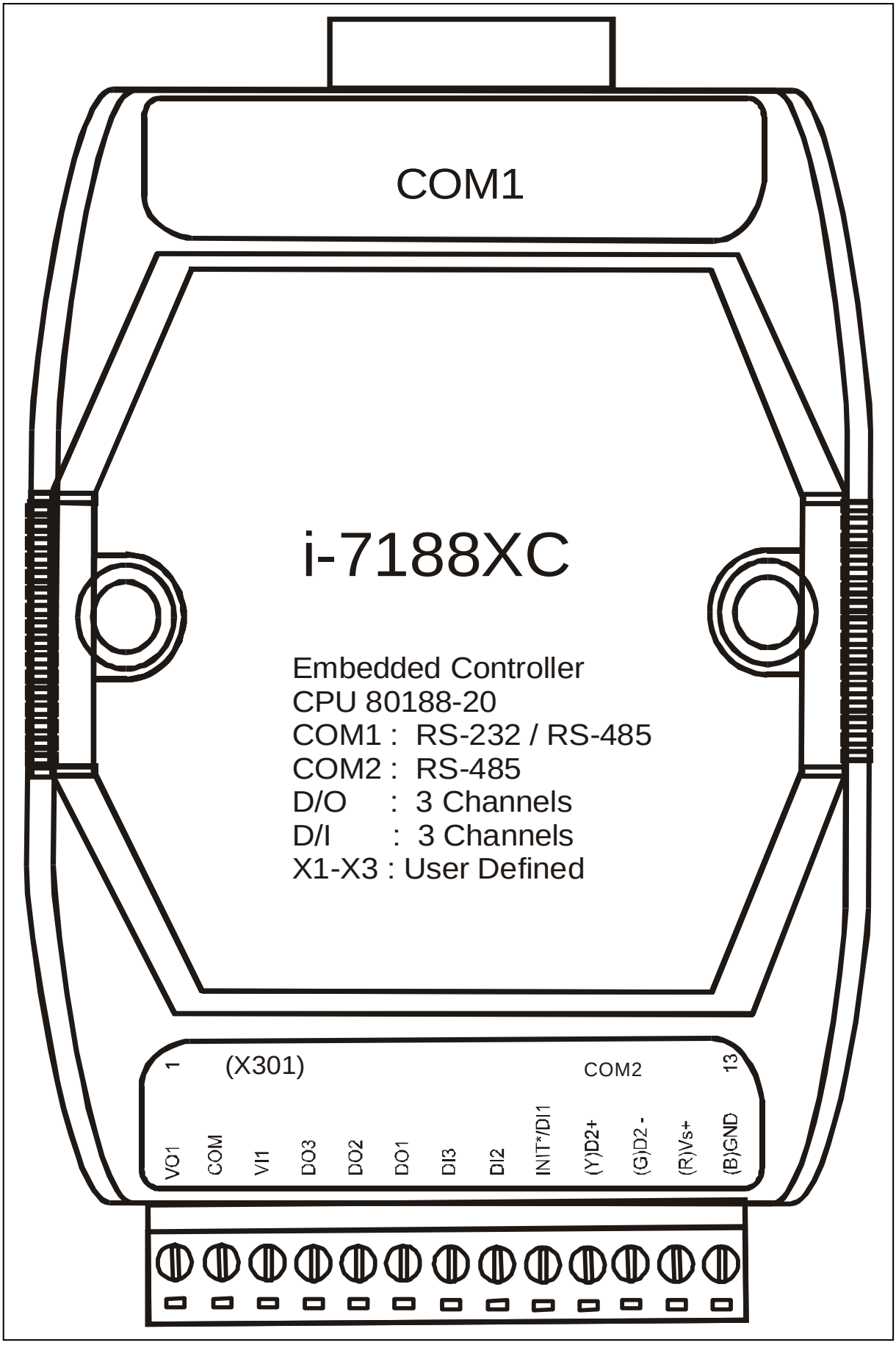
3.11.1 Specifications

- 1 channel of 12 bit D/A (0-4.095v)
- 1 channel of 12 bit A/D (0-2.5v)
- For 7188XC series

3.11.2 Pin Assignment & Jumper Setting



- **J1:** I/O expansion bus, connect to J1 of 7188XC
- **J2:** I/O expansion bus, connect to J2 of 7188XC
- **J7:** A/D + D/A
- **J5:** The pin assignment is given as follows:


COM1
i-7188XC
Embedded Controller
CPU 80188-20
COM1 : RS-232 / RS-485
COM2 : RS-485
D/O : 3 Channels
D/I : 3 Channels
X1-X3 : User Defined
1
(X301)
COM2
13
VO1
COM
VI1
DO3
DO2
DO1
DI3
DI2
INIT*/DI1
(Y)D2+
(G)D2 -
(R)Vs+
(B)GND

3.11.3 Programming

void AnalogOutput(int DataIn)

DataIn = 0 – 4095 (Note 4095→ 4.095V)

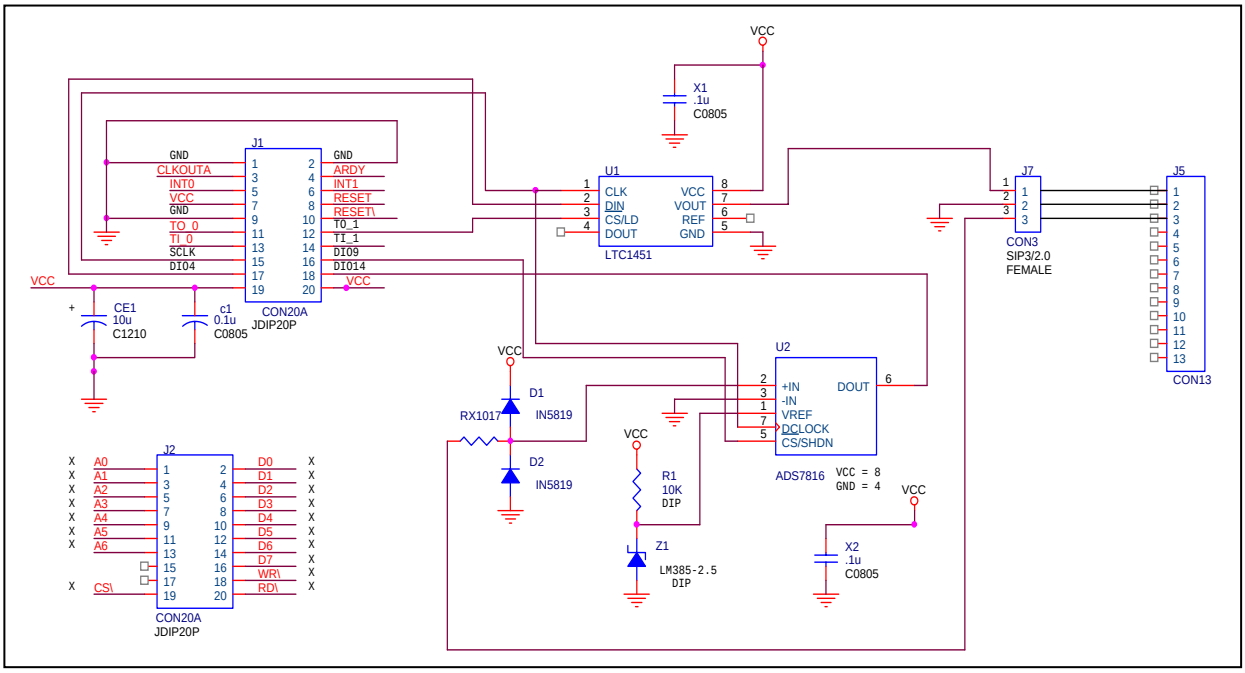
int AnalogIn(void)

Return value= 0 - 4095

Mapping formula: Vref / 4096 (Note: Vref=2.5v)

- Refer to C:\7188xc\demo\ioexpbus\X301*.* for demo program

3.11.4 Circuit Diagram

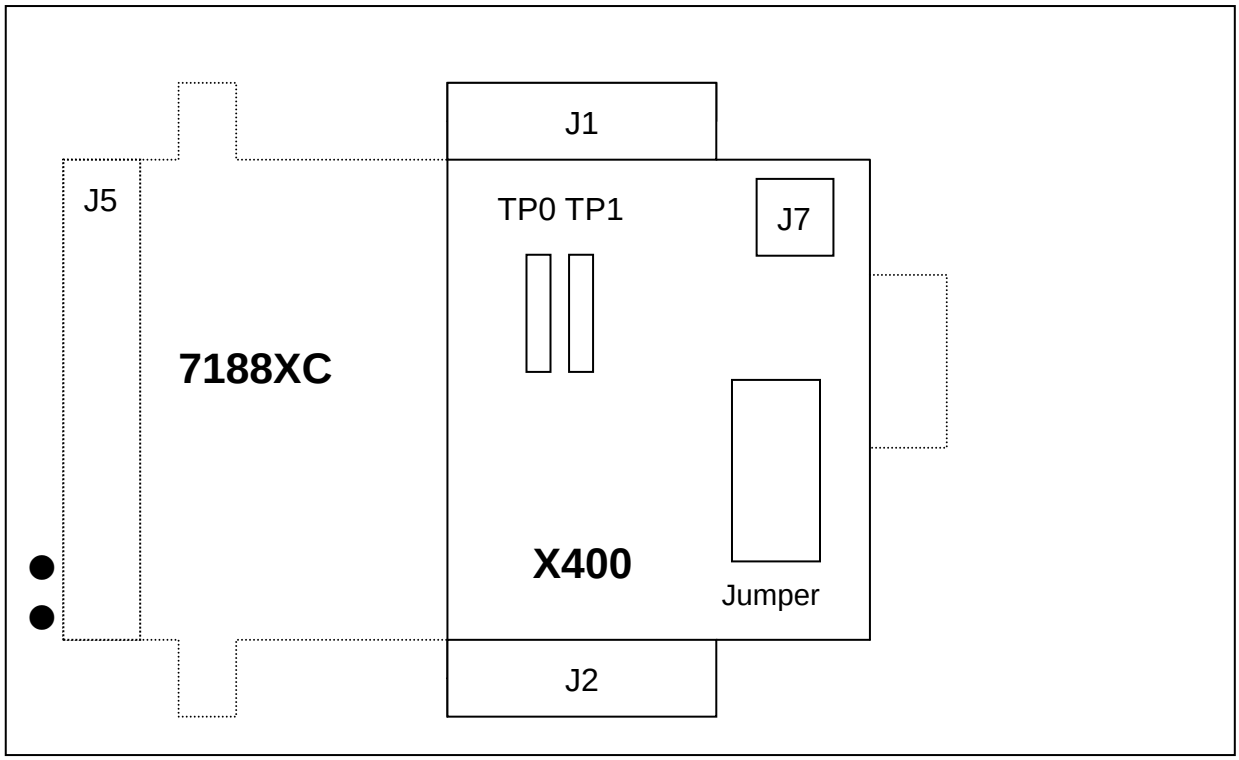


3.12 X400 Timer/Counter * 3

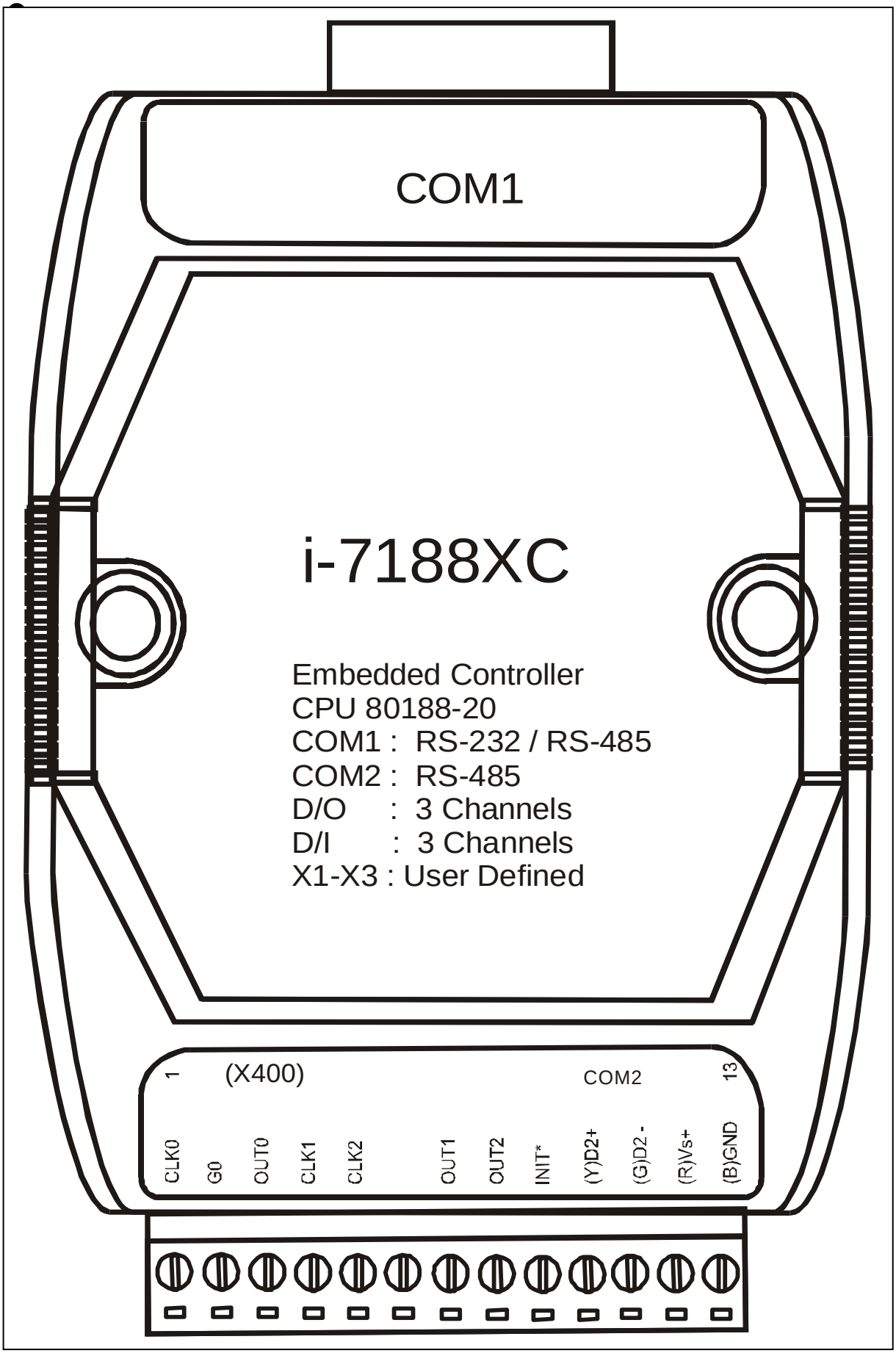
3.12.1 Specifications

- 3 channels of 16 bit timer/counter
- For 7188XC series

3.12.2 Pin Assignment & Jumper Setting



- **J1:** I/O expansion bus, connect to J1 of 7188XC
- **J2:** I/O expansion bus, connect to J2 of 7188XC
- **J7:** for counter-0
- **TP0:** Original function on 7188XC
- **TP1**: for counter1, counter2
- **J5:** The pin assignment is given as follows:


COM1
i-7188XC
Embedded Controller
CPU 80188-20
COM1 : RS-232 / RS-485
COM2 : RS-485
D/O : 3 Channels
D/I : 3 Channels
X1-X3 : User Defined
1
(X400)
COM2
13
CLK0
G0
OUT0
CLK1
CLK2
OUT1
OUT2
INIT*
(Y)D2+
(G)D2 -
(R)Vs+
(B)GND

Jumper setting for 8254:

●	1-2 ON	2-3 ON
CLK0	T1 → CLK0=TO_0	T1 → CLK0=pin1 of J5
G0	T2 → G0=always High	T2 → G0=pin2 of J5
OUT0	OUT0 to INT0 & pin3 of J5	
CLK1	T4 → CLK1=TO_1	T4 → CLK0=pin4 of J5
G1	Always High	
OUT1	OUT1 to T3.1 & T5.1 & T6.1	
CLK2	T3 → CLK2=OUT1	T3 → CLK2=pin5 of J5
G2	Always High	
OUT2	OUT2 to T5.3 & T7.1	

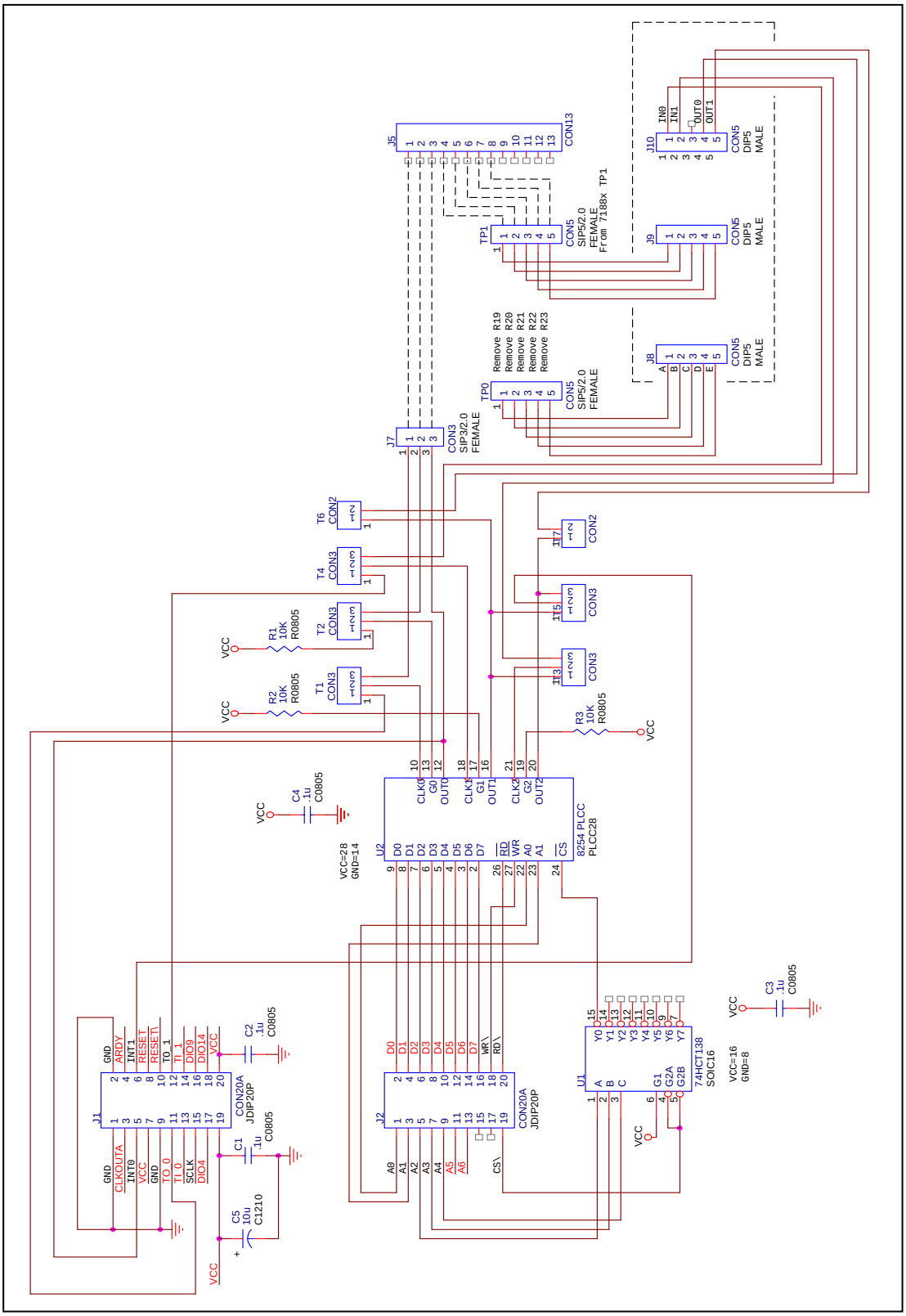
- T1 is used to select internal TO_0 or external signal for CLK0
- T2 is used to select High or external signal for G0
- T3 is used to control 16-bit/32-bit counter. 1-2 select 32-bits counter, 2-3 select two 16-bit counters
- T4 is used to select internal TO_1 or external signal for CLK1
- T5 is used to select OUT1 or OUT2 to INT1
- T6 is used to select OUT1 to pin-7 of J5
- T7 is used to select OUT2 to pin-8 of J5

Refer to Sec. 3.15.4 for more information about jumper setting

3.12.3 Programming

- Refer to C:\7188xc\demo\ioexpbus\X400*.* for demo program

3.12.4 Circuit Diagram

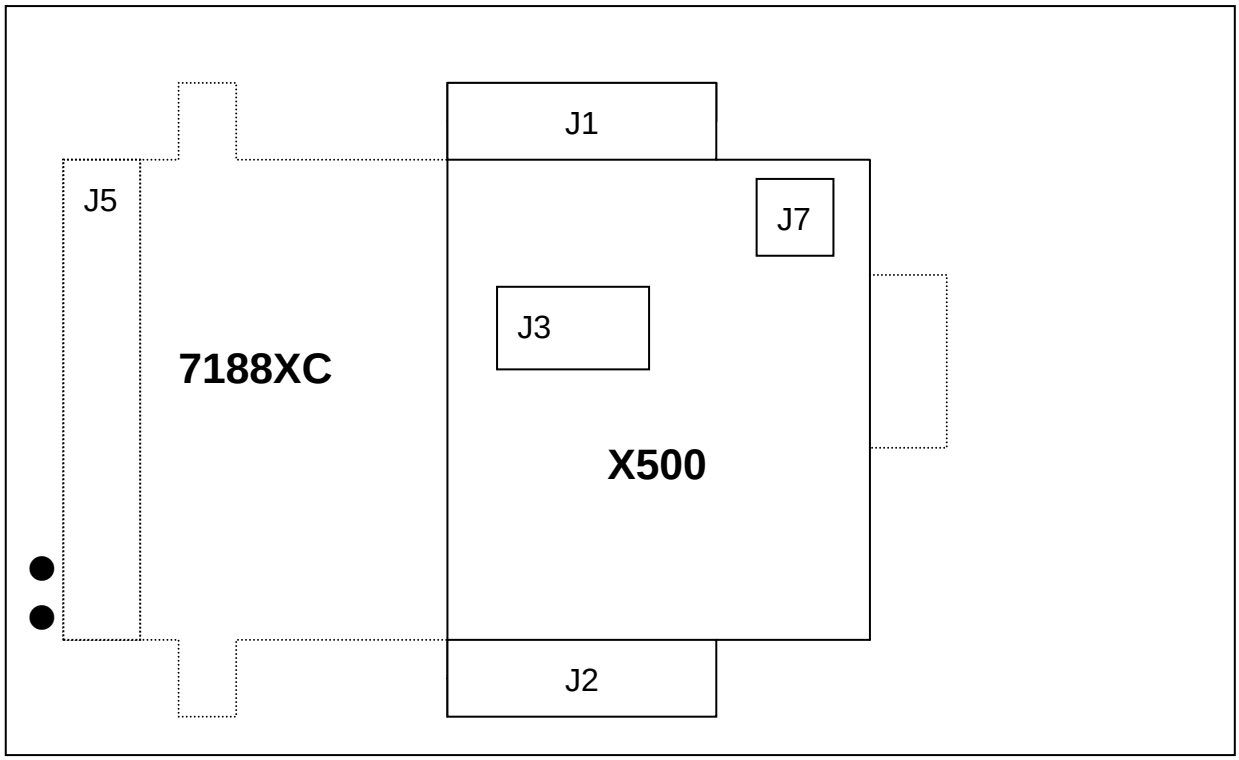


3.13 X500 RS232 * 1

3.13.1 Specifications

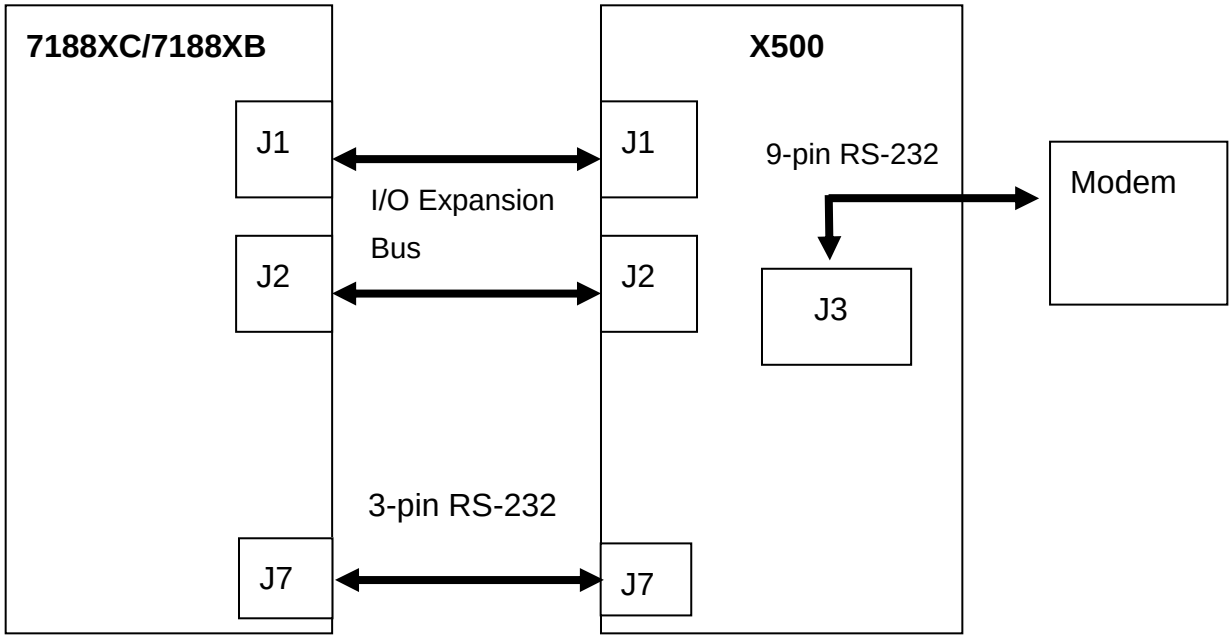
- 1 channel of RS-232, modem control, 115.2K
  (RI, DSR, DCD, RTS, CTS, TXD, RXD, GND)
- For 7188XC series
- Compatible to **COM3** of 7188X software library

3.13.2 Pin Assignment & Jumper Setting



- **J1:** I/O expansion bus, connect to J1 of 7188XC
- **J2:** I/O expansion bus, connect to J2 of 7188XC
- **J7:** Three wires of RS-232 (RXD, TXD, GND)
- **J3:** 9-pin connector of RS-232, connect to modem
- **J5:** The pin assignment is given as follows:

Block Diagram

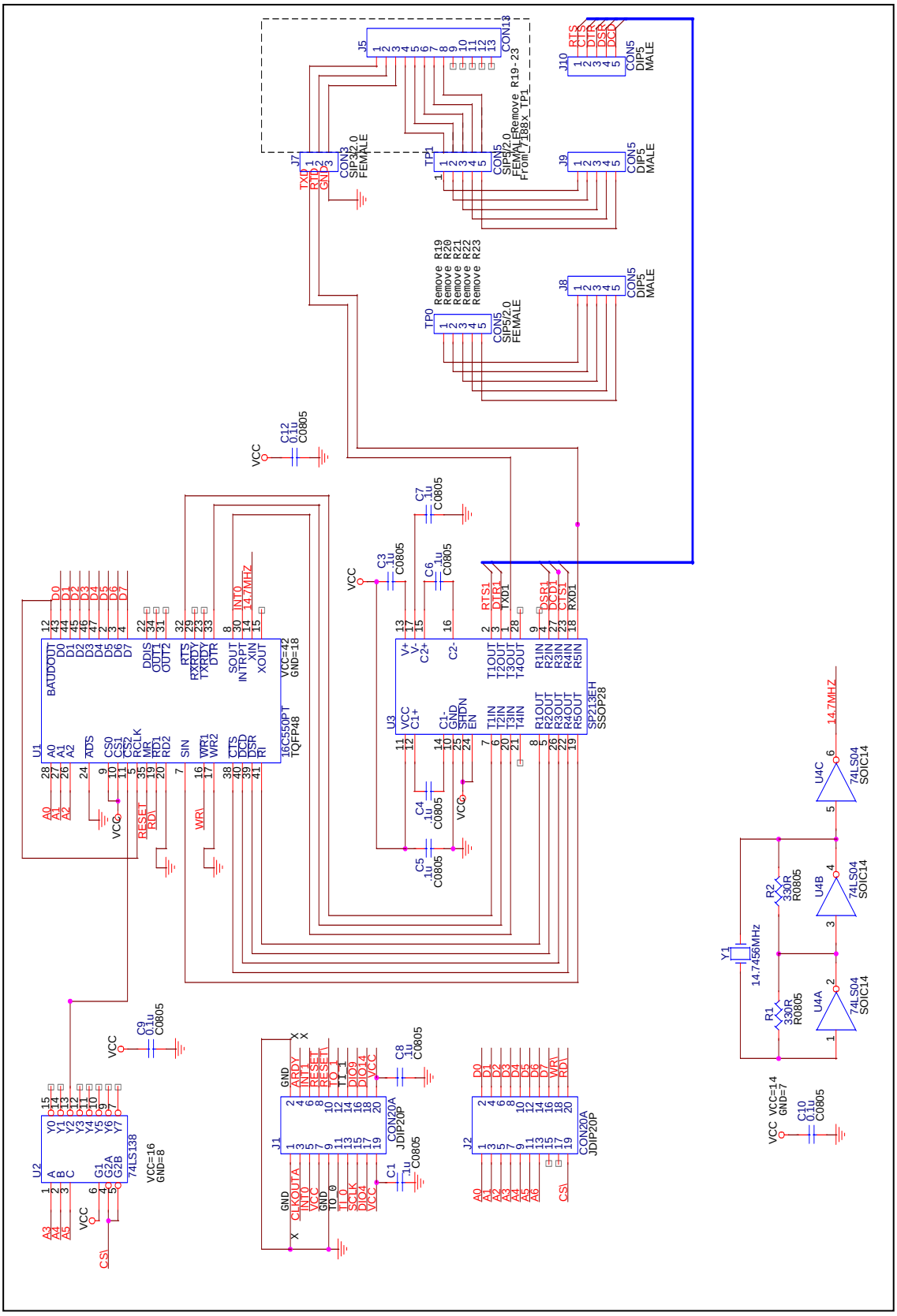


3.13.3 Programming

- Refer to C:\7188xc\demo\ioexpbus\X500*.* for demo program

int InstallCom3(unsigned long baud, int data, int parity, int stop);
int RestoreCom3(void);
int IsCom3(void);
int ToCom3(int data);
int ToCom3Str(char *str);
int ToCom3Bufn(char *buf,int no);
int printCom3(char *fmt,...);
void ClearTxBuffer3(void);
int SetCom3FifoTriggerLevel(int level);
int SetBaudrate3(unsigned long baud);
int ReadCom3(void);
int ClearCom3(void);
int DataSizeInCom3(void);
int WaitTransmitOver3(void);
int IsTxBufEmpty3(void);
int IsCom3OutBufEmpty(void);

3.13.4 Circuit Diagram

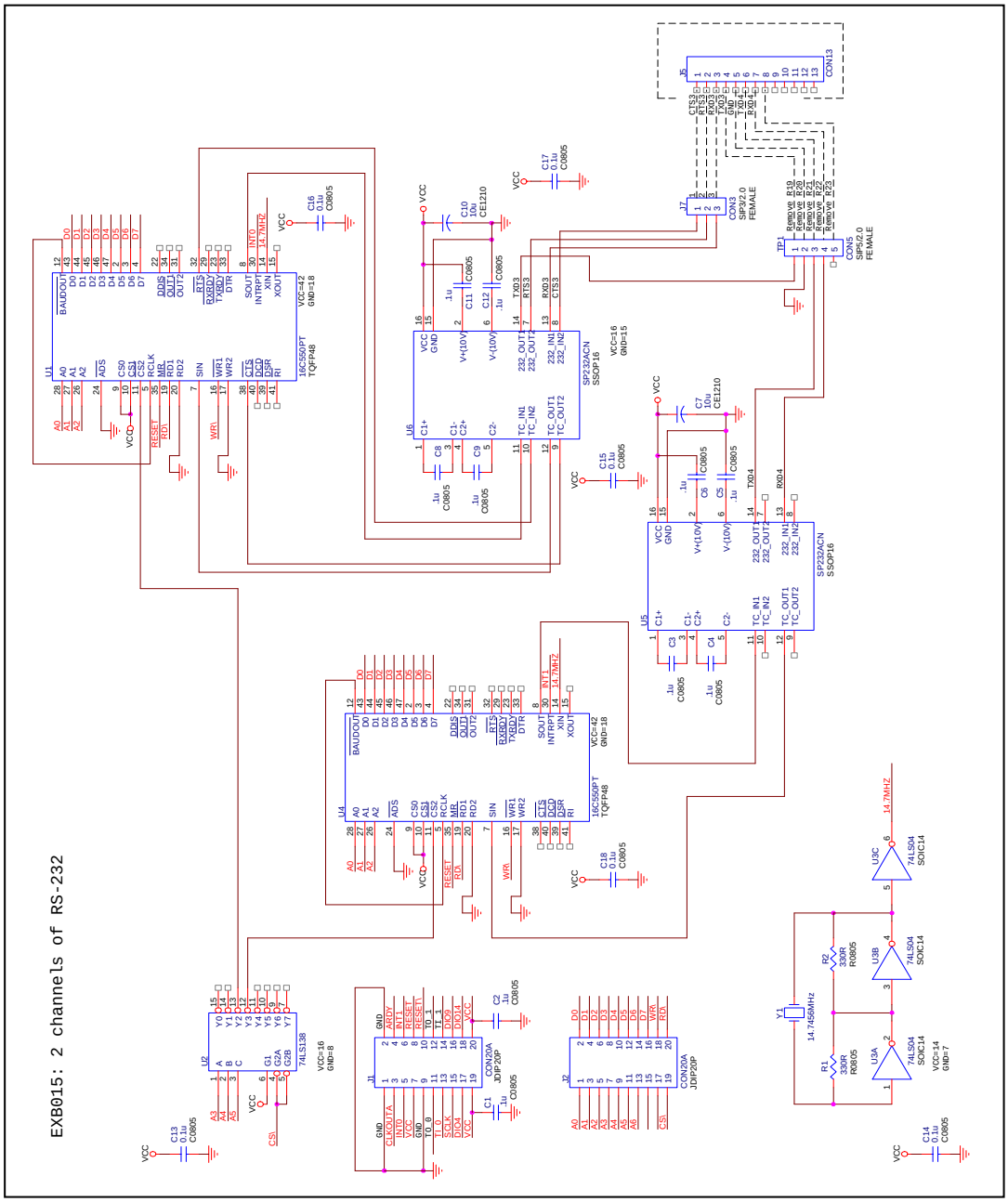


3.14 X501/X502

3.14.1 Specifications

- X501 is designed for 7522 **(COM3)**, (RTS, CTS, TXD, RXD, GND)
- X502 is designed for 7523 **(COM3 & COM4)**
  COM3 (RTS, CTS, TXD, RXD, GND), **COM4** (TXD, RXD, GND)
- Refer to “7521/7522/7523 Software User’s Manual” for more information

3.14.2 Circuit Diagram

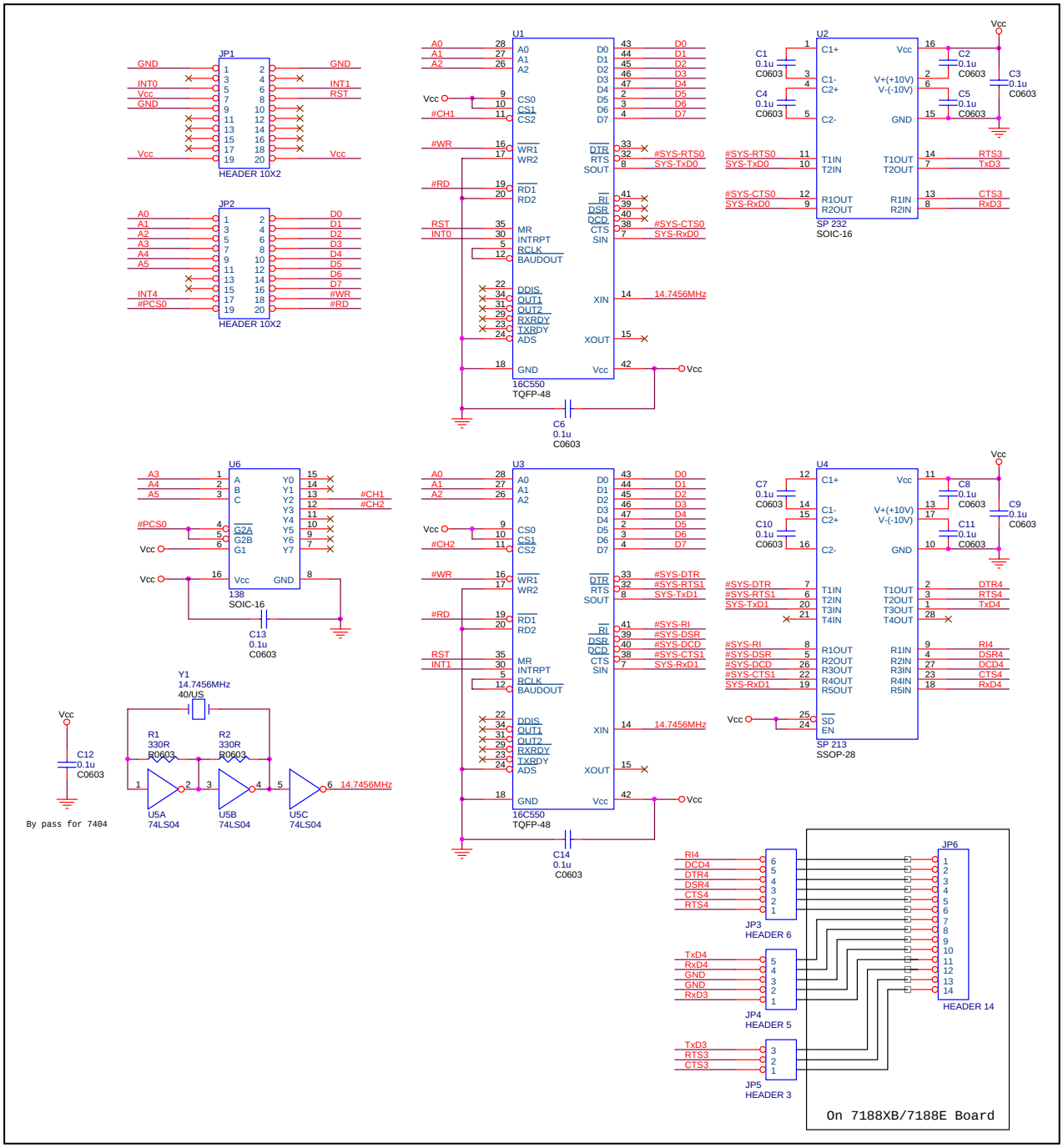


3.15 X503/X504

3.15.1 Specifications

- X503 & X504 are designed for 7188XB/7188E
- X503: COM3 only; X504: COM3 & COM4
- Compatible to **COM3 & COM4** of 7188X software library

3.15.2 Circuit Diagram



3.16 X600 ~ X603

3.16.1 Specifications

- X600: storage flash, 4M bytes
- X601: storage flash, 8M bytes
- X602: storage flash, 16M bytes
- X603: storage flash, 32M bytes
- Refer to C:\7188xc\demo\ioexpbus\X600*.* for demo program

3.16.2 Software Library

```
int  X600_Init(int wBaseAddr, int wType);
int  X600_Reset_FLASH(void);
int  X600_WP_FLASH(char wp);
void X600_Read_FLASH_ID(int *maker, int *device);
void X600_Read_FLASH_Status(int *status);
int  X600_MarkBadPage(unsigned int wAddr);
int  X600_Erase_FLASH(unsigned int wAddr);
int  X600_Erase_FLASH_Unconditional(unsigned int wAddr);
int  X600_Write_FLASH(unsigned int wAddr, char buf1[], char buf2[]);
int  X600_Read_FLASH(unsigned int wAddr, char buf1[], char buf2[]);
```

3.17 X607

3.17.1 Specifications

- 128K bytes SRAM, battery backup
- Refer to C:\7188xc\demo\ioexpbus\X607*.* for demo program

3.17.2 Circuit Diagram